Golem / Talos (L14 / L15 Gen3)
AMD Ryzen Barcelo Schematics

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

DY	*DUMMY, NOT ASM, not assemble*
ZZ	*For Test Piont /Hole /ShortPad*
PCB_IDX_X	*PCB ID for SW Team (PCB Number)*
SKU_ID	*SKU ID for SW Team (CPU Type)*
PSL	*KBC PSL Model Control (Always ASM)*
HDT	*Debug Function*
MS/ NON_MS	*Modern stand by/ NON Modern stand by*
TPM/ TCM	*TPM Selection for SW Team (TCM will be DY)* *TCM Selection for SW Team (TPM will be DY)*
DASH/ NON_DASH	*BOM control by CPU Type (pro/ non pro)*

L14 L15 LAN

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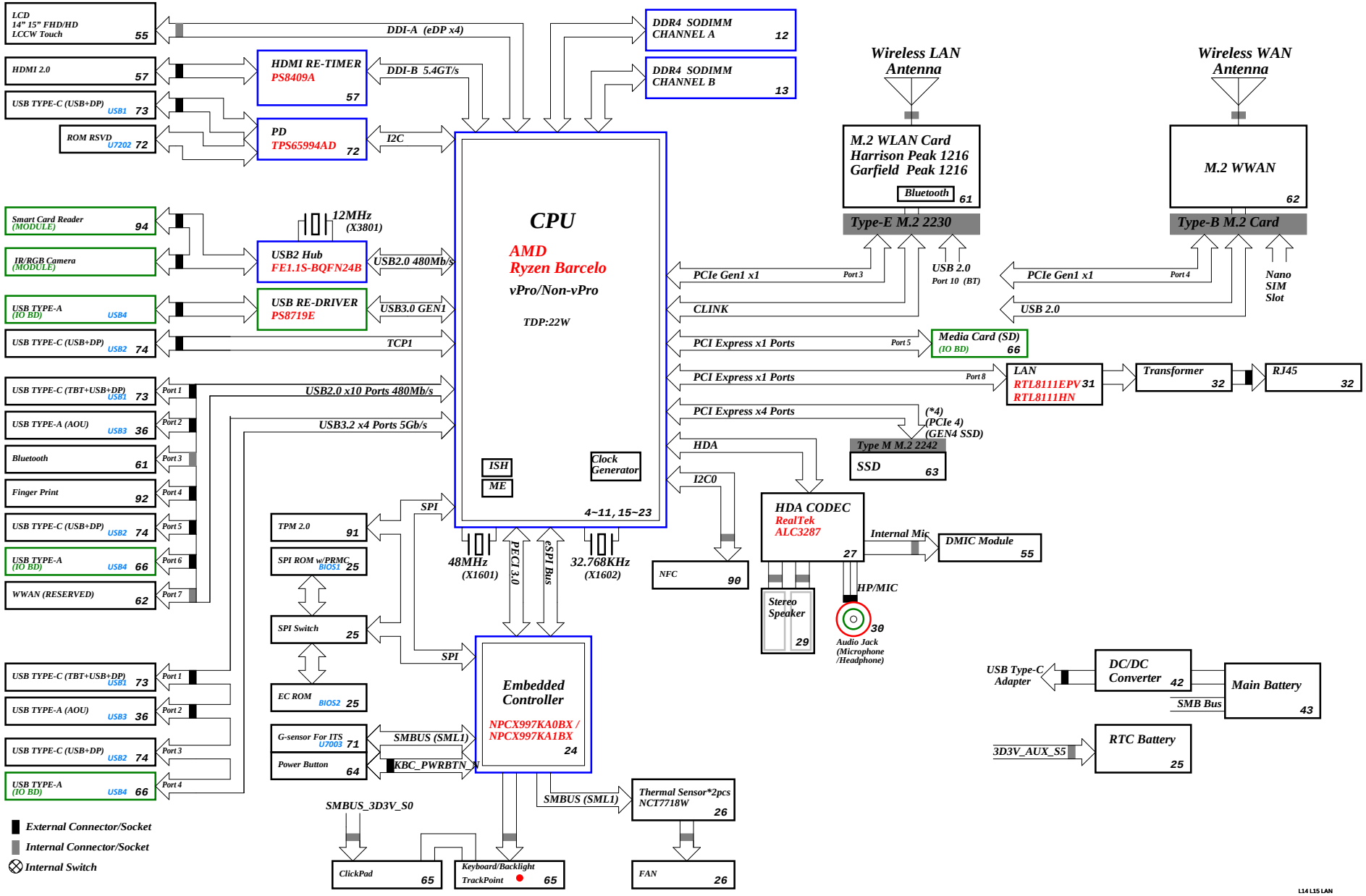
Title: **COVER PAGE**

Size: A3 | Document Number: **L14 L15 AMD** | Rev: **-1**

Date: Wednesday, April 06, 2022 | Sheet 1 of 106

Golem / Talos (L14 / L15 Gen3) AMD Ryzen Barcelo Block Diagram

Project code : 4PD0PZ010001 / 4PD0PZ01F001
Project name : LG4-1 AMD / LT5-1 AMD
PCB P/N : 213039
Revision : -1



PCB Layer Stackup

FR4 8 Layers < 8-1.0-15p >

- L1: Component (TOP)
- L2: GND
- L3: Signal
- L4: GND
- L5: Signal
- L6: Signal
- L7: GND
- L8:Component (BOTTOM)

Battery Charger BQ25710RSNR		44
20V_VINT_IN	19V_DCBATOUT BT+	
DC/DC 5V TPS51395PRJER		45
19V_DCBATOUT	5V_S5 5V_AUX_S5	
DC/DC 3D3V TPS51393PRJER		45
19V_DCBATOUT	3D3V_S5 3D3V_AUX_S5	
DC/DC VCORE MP2945GU		46
DC/DC 1V_CPU_CORE MP86901		47
19V_DCBATOUT	1V_CPU_CORE	
DC/DC 1V_VDDCR_SOC MP86901		48
19V_DCBATOUT	1V_VDDCR_SOC	
		50
DC/DC 1D2V_S3 RT8231AGQW		51
19V_DCBATOUT	1D2V_S3	
DC/DC 0D6V_VREF_S0 RT8231AGQW		51
1D2V_S3	0D6V_VREF_S0	
DC/DC 2D5V_S5 APL5934KAI		51
5V_S5	2D5V_S3	
DC/DC 0D75V_S5 RT5753ALGQW		52
3D3V_S5	0D75V_S5	
DC/DC 0D75V_S0 RT5753ALGQW		52
3D3V_S5	0D75V_S0	
DC/DC 1D8V_SUS SY8386RHC		
3D3V_S5	1D8V_S5	53

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Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
A2	L14 L15 AMD	-1

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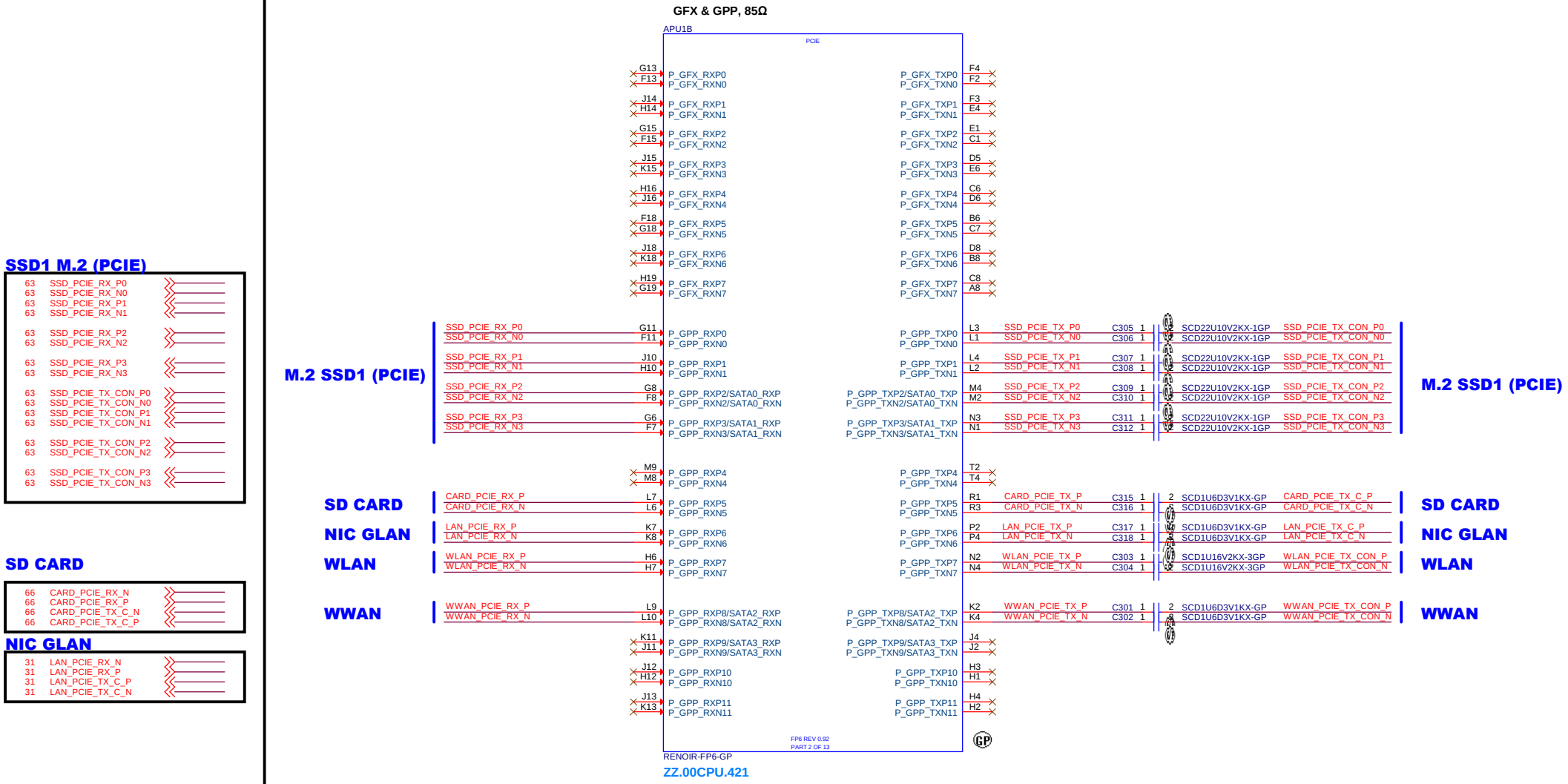

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Title: ***CPU (PCIE/SATA)***

Size	Document Number	Rev
A3	**L14 L15 AMD**	-1

Date: Wednesday, April 06, 2022 Sheet 3 of 106

BLANK

L14 L15 LAN

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Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 4 of 106

APU Type 2 does not support Channel A

ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

DM, DQ & DQS on the same layer

APU1A
MEMORY A

M_A_DQS_DN[7:0] 12
M_A_DQS_DP[7:0] 12
M_A_DQ[63:0] 12
M_A_A[16:0] 12

12 M_A_A0
12 M_A_A1
12 M_A_A2
12 M_A_A3
12 M_A_A4
12 M_A_A5
12 M_A_A6
12 M_A_A7
12 M_A_A8
12 M_A_A9
12 M_A_A10
12 M_A_A11
12 M_A_A12
12 M_A_A13
12 M_A_A14
12 M_A_A15
12 M_A_A16

12 M_A_BA0
12 M_A_BA1
12 M_A_BG0
12 M_A_BG1
12 M_A_ACT_N
12 M_A_DM0
12 M_A_DM1
12 M_A_DM2
12 M_A_DM3
12 M_A_DM4
12 M_A_DM5
12 M_A_DM6
12 M_A_DM7

12 M_A_CLK_P0
12 M_A_CLK_N0
12 M_A_CLK_P1
12 M_A_CLK_N1

12 M_A_CS0_N
12 M_A_CS1_N
12 M_A_CKE0
12 M_A_CKE1
12 M_A_ODT0
12 M_A_ODT1
12 M_A_ALERT_N
12 SM_DRAMRST_N_A
12 M_A_PARITY
12 M_A_EVENT_N

M_A_A0	AK26	MA_ADD0/RSVD
M_A_A1	AG24	MA_ADD1/RSVD
M_A_A2	AG23	MA_ADD2/MAB_CA0
M_A_A3	AG26	MA_ADD3/MAA_CA4
M_A_A4	AG27	MA_ADD4/MAA_CA5
M_A_A5	AF21	MA_ADD5/MAA_CA3
M_A_A6	AF22	MA_ADD6/MAA_CA2
M_A_A7	AF25	MA_ADD7/RSVD
M_A_A8	AF24	MA_ADD8/RSVD
M_A_A9	AE21	MA_ADD9/RSVD
M_A_A10	AL21	MA_ADD10/MAB_CS_L1
M_A_A11	AF27	MA_ADD11/MAA_CKE1
M_A_A12	AE23	MA_ADD12/MAA_CKE0
M_A_A13	AM23	MA_ADD13_BANK2/RSVD
M_A_A14	AM21	MA_WE_L_ADD14/MAB_CKE1
M_A_A15	AL27	MA_CAS_L_ADD15/RSVD
M_A_A16	AL24	MA_RAS_L_ADD16/MAB_CKE0
M_A_BA0	AL22	MA_BANK0/MAB_CS_L0
M_A_BA1	AK27	MA_BANK1/MAB_CA1
M_A_BG0	AE27	MA_BG0/MAA_CS_L1
M_A_BG1	AE26	MA_BG1/MAA_CS_L0
M_A_ACT_N	AD22	MA_ACT_L/RSVD
M_A_DM0	L27	MA_DM0/MAA_DM1
M_A_DM1	N23	MA_DM1/MAA_DM0
M_A_DM2	R27	MA_DM2/MAA_DM2
M_A_DM3	Y24	MA_DM3/MAA_DM3
M_A_DM4	AP27	MA_DM4/MAB_DM2
M_A_DM5	AW23	MA_DM5/MAB_DM3
M_A_DM6	AT21	MA_DM6/MAB_DM1
M_A_DM7	AV18	MA_DM7/MAB_DM0
	W24	RSVD_52
M_A_DQS_DP0	M25	MA_DQS_H0/MAA_DQS_H1
M_A_DQS_DN0	M24	MA_DQS_L0/MAA_DQS_L1
M_A_DQS_DP1	P22	MA_DQS_H1/MAA_DQS_H0
M_A_DQS_DN1	P21	MA_DQS_L1/MAA_DQS_L0
M_A_DQS_DP2	T24	MA_DQS_H2/MAA_DQS_H2
M_A_DQS_DN2	R24	MA_DQS_L2/MAA_DQS_L2
M_A_DQS_DP3	AA21	MA_DQS_H3/MAA_DQS_H3
M_A_DQS_DN3	Y21	MA_DQS_L3/MAA_DQS_L3
M_A_DQS_DP4	AP23	MA_DQS_H4/MAB_DQS_H2
M_A_DQS_DN4	AP24	MA_DQS_L4/MAB_DQS_L2
M_A_DQS_DP5	AW22	MA_DQS_H5/MAB_DQS_H3
M_A_DQS_DN5	AV22	MA_DQS_L5/MAB_DQS_L3
M_A_DQS_DP6	AT20	MA_DQS_H6/MAB_DQS_H1
M_A_DQS_DN6	AR20	MA_DQS_L6/MAB_DQS_L1
M_A_DQS_DP7	AR18	MA_DQS_H7/MAB_DQS_H0
M_A_DQS_DN7	AT18	MA_DQS_L7/MAB_DQS_L0
	Y26	RSVD_58
	Y27	RSVD_59
M_A_CLK_P0	AJ25	MA_CLK_H0/MAA_CKT
M_A_CLK_N0	AJ24	MA_CLK_L0/MAA_CKC
M_A_CLK_P1	AJ22	MA_CLK_H1/MAB_CKT
M_A_CLK_N1	AJ21	MA_CLK_L1/MAB_CKC
M_A_CS0_N	AL25	MA_CS_L0/MAB_CA2
M_A_CS1_N	AM26	MA_CS_L1/MAB_CA5
M_A_CKE0	AD24	MA_CKE0/MAA_CA1
M_A_CKE1	AD25	MA_CKE1/MAA_CA0
M_A_ODT0	AM24	MA_ODT0/MAB_CA3
M_A_ODT1	AM27	MA_ODT1/MAB_CA4
M_A_ALERT_N	AE24	MA_ALERT_L/TEST31A
M_A_EVENT_N	AK23	MA_EVENT_L
SM_DRAMRST_N_A	AD27	MA_RESET_L

MA_DATA0/MAA_DATA8	K27	M_A_DQ0
MA_DATA1/MAA_DATA9	L26	M_A_DQ1
MA_DATA2/MAA_DATA13	N26	M_A_DQ2
MA_DATA3/MAA_DATA12	N27	M_A_DQ3
MA_DATA4/MAA_DATA11	G27	M_A_DQ4
MA_DATA5/MAA_DATA10	H27	M_A_DQ5
MA_DATA6/MAA_DATA15	M27	M_A_DQ6
MA_DATA7/MAA_DATA14	N24	M_A_DQ7
MA_DATA8/MAA_DATA0	L23	M_A_DQ8
MA_DATA9/MAA_DATA1	N21	M_A_DQ9
MA_DATA10/MAA_DATA5	T21	M_A_DQ10
MA_DATA11/MAA_DATA4	T22	M_A_DQ11
MA_DATA12/MAA_DATA7	M22	M_A_DQ12
MA_DATA13/MAA_DATA6	L24	M_A_DQ13
MA_DATA14/MAA_DATA2	R21	M_A_DQ14
MA_DATA15/MAA_DATA3	R23	M_A_DQ15
MA_DATA16/MAA_DATA17	P24	M_A_DQ16
MA_DATA17/MAA_DATA16	R26	M_A_DQ17
MA_DATA18/MAA_DATA21	T27	M_A_DQ18
MA_DATA19/MAA_DATA20	V27	M_A_DQ19
MA_DATA20/MAA_DATA19	P25	M_A_DQ20
MA_DATA21/MAA_DATA18	P27	M_A_DQ21
MA_DATA22/MAA_DATA23	V23	M_A_DQ22
MA_DATA23/MAA_DATA22	T25	M_A_DQ23
MA_DATA24/MAA_DATA30	W22	M_A_DQ24
MA_DATA25/MAA_DATA31	Y23	M_A_DQ25
MA_DATA26/MAA_DATA26	AC24	M_A_DQ26
MA_DATA27/MAA_DATA27	AC23	M_A_DQ27
MA_DATA28/MAA_DATA28	V21	M_A_DQ28
MA_DATA29/MAA_DATA29	W21	M_A_DQ29
MA_DATA30/MAA_DATA24	AA24	M_A_DQ30
MA_DATA31/MAA_DATA25	AA22	M_A_DQ31
MA_DATA32/MAB_DATA17	AP26	M_A_DQ32
MA_DATA33/MAB_DATA16	AN24	M_A_DQ33
MA_DATA34/MAB_DATA21	AR25	M_A_DQ34
MA_DATA35/MAB_DATA20	AU26	M_A_DQ35
MA_DATA36/MAB_DATA19	AN25	M_A_DQ36
MA_DATA37/MAB_DATA18	AN27	M_A_DQ37
MA_DATA38/MAB_DATA23	AR27	M_A_DQ38
MA_DATA39/MAB_DATA22	AU27	M_A_DQ39
MA_DATA40/MAB_DATA30	AV25	M_A_DQ40
MA_DATA41/MAB_DATA31	AW25	M_A_DQ41
MA_DATA42/MAB_DATA26	AV20	M_A_DQ42
MA_DATA43/MAB_DATA27	AW20	M_A_DQ43
MA_DATA44/MAB_DATA28	AV27	M_A_DQ44
MA_DATA45/MAB_DATA29	AW26	M_A_DQ45
MA_DATA46/MAB_DATA24	AU21	M_A_DQ46
MA_DATA47/MAB_DATA25	AW21	M_A_DQ47
MA_DATA48/MAB_DATA11	AT22	M_A_DQ48
MA_DATA49/MAB_DATA10	AP21	M_A_DQ49
MA_DATA50/MAB_DATA14	AN19	M_A_DQ50
MA_DATA51/MAB_DATA15	AN18	M_A_DQ51
MA_DATA52/MAB_DATA12	AU23	M_A_DQ52
MA_DATA53/MAB_DATA13	AR22	M_A_DQ53
MA_DATA54/MAB_DATA9	AN20	M_A_DQ54
MA_DATA55/MAB_DATA8	AP19	M_A_DQ55
MA_DATA56/MAB_DATA6	AT19	M_A_DQ56
MA_DATA57/MAB_DATA7	AW18	M_A_DQ57
MA_DATA58/MAB_DATA2	AU16	M_A_DQ58
MA_DATA59/MAB_DATA3	AW16	M_A_DQ59
MA_DATA60/MAB_DATA4	AW19	M_A_DQ60
MA_DATA61/MAB_DATA5	AU19	M_A_DQ61
MA_DATA62/MAB_DATA1	AP16	M_A_DQ62
MA_DATA63/MAB_DATA0	AT16	M_A_DQ63
RSVD_54	W27	
RSVD_53	W25	
RSVD_68	AC26	
RSVD_69	AC27	
RSVD_49	V26	
RSVD_48	V24	
RSVD_63	AA27	
RSVD_62	AA25	
MA_PAROUT/RSVD	AK24	M_A_PARITY
M_DDR4 M_LPDDR4	AN21	
	AN22	

FP6 REV 0.92
PART 1 OF 13

RENOIR-FP6-GP

ZZ.00CPU.421

1D2V_S3

1D2V_S3 — 1 — R502 1KR2J-1-GP — M_A_ALERT_N

1D2V_S3 — 1 — R501 1KR2J-1-GP — M_A_EVENT_N

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Title: CPU (DDR4_CHA)

Size: A3 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 5 of 106

ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

ADD and CLK on the sam layer

DM, DQ & DQS on the same layer

DM, DQ & DQS on the same layer

Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK	BG	
Command	RAS_L	CAS_L	WE_L	ACT
Control	CKE	ODT	CS_L	
Data	Data	DM	DQS	
Misc. M_PAROUT	M_RESET_L	M_EVENT_L	M_ALERT	

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APU1I
MEMORY B
RENOIR-FP6-GP
FP6 REV 0.92
PART 9 OF 13
ZZ.00CPU.421

1D2V_S3
R602
1KR2J-1-GP
M_B_ALERT_N

1D2V_S3
R601
1KR2J-1-GP
M_B_EVENT_N

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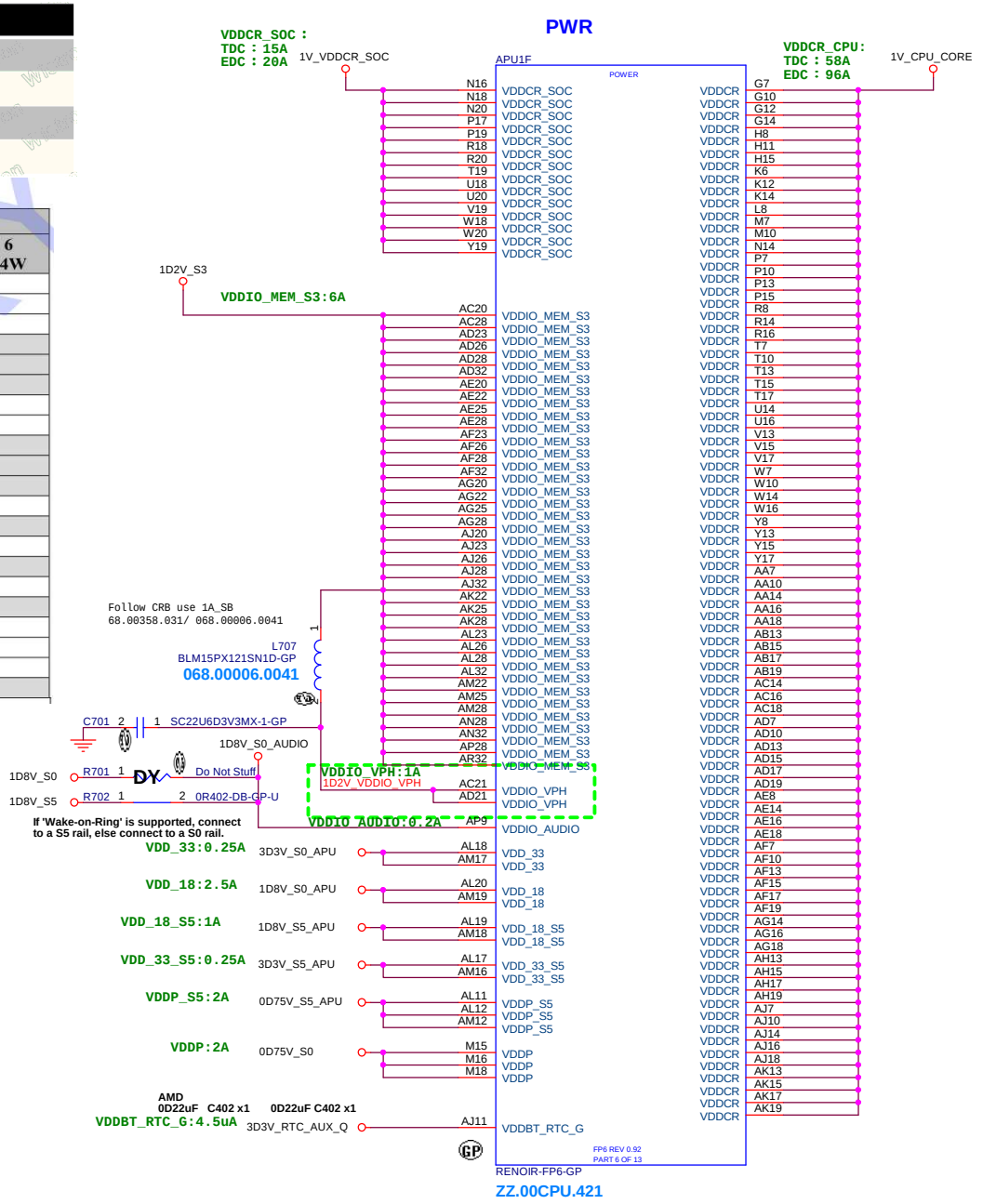
Title: CPU (DDR4_CHB)
Size: A3
Document Number: L14 L15 AMD
Rev: -1
Date: Wednesday, April 06, 2022
Sheet 6 of 106

SVI	FP4 – Bristol Ridge	FP5 – Raven Ridge
Supply 1	VDDCR_CPU – x86 Cores	VDDCR_VDD – x86 Cores, GPU
Supply 2	VDDCR_NB – Rest Of Chip	VDDCR_SOC – Rest Of Chip
Supply 3	VDDCR_GFX – GPU	N/A
Sum@15W	TDC: 56A, EDC: 87A	TDC: 45A, EDC: 58A

Table 5. FP6 Processor Voltage Supply Currents

Supply [1]	Nominal Voltage at Pkg Ball (V) [2]	Condition	SYSTEM_CONFIGURATION 1 10W	2 15W	3 25W	4 35W	5 45W	6 54W
VDDCR_VDD	Variable (0.65–TBD)[5]	TDC [3]	20	33	44	51	58	
		EDC	34	50	70	90	96	
		Max Loadstep [4]	29	43	65	76	84	
VDDCR_SOC	Variable (0.7–TBD)[5]	TDC [3]	10	13			15	
		EDC	13	17			20	
		Max Loadstep [4]						
VDDIO_MEM_S3[6]	1.10	TDC	6.00					
	1.20	TDC	6.00					
VDDIO_VPH[7]	1.10	TDC	1.00					
	1.20	TDC	1.00					
	1.80	TDC	1.00					
VDDP	0.75	TDC	2.00					
VDDP_S5	0.75	TDC	2.00					
VDD_18	1.80	TDC	2.50					
VDD_18_S5	1.80	TDC	1.00					
VDD_33	3.30	TDC	0.25					
VDD_33_S5	3.30	TDC	0.25					
VDDIO_AUDIO	1.20	TDC	0.20					
	1.50	TDC	0.20					
	1.80	TDC	0.20					
VDDBT_RTC_G	3.00	TDC	4.5µA					



15.3.5 VDDIO_VPH Power Delivery and Decoupling

VDDIO_VPH is the dedicated supply voltage for DisplayPort 0 and PCIe phys. When DisplayPort 0 is used for eDP, the source of VDDIO_VPH can be the same source as VDDIO_MEM_S3. This allows lower power and better battery life. When DisplayPort 0 is used for DP or TMDS, the source of VDDIO_VPH can be the same source as VDD_18.

L14 L15 LAN

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER)

Size: A3 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 7 of 106

DISPLAY/SVI/JTAG/TEST

APU Type I(CZ): 1D8V
APU Type II(CZ-L): 3D3V

APU Type I 1D8V
APU Type II 3D3V

PINOUT	Description
DP_BLON	BL_ENABLE
DP_DIGON	LCD_VCC_ENABLE
DP_VARY_BL	BL_PWM

DisplayPort	Device
0	eDP
1	HDMI
2	TYPEC1
3	TYPEC2

eDP

55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N1
24 PANEL_BLEN
55 EDP_VDD_EN
55 PANEL_BKLTCTL
55 eDP_AUX_CPU_P
55 eDP_AUX_CPU_N
55 EDP_HPD_CPU

HDMI

57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P3
57 HDMI_DDI_TX_N3
57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_HPD_CPU

HDT

68 APU_TDI
68 APU_TDO
68 APU_TCK
68 APU_TMS
68 APU_TRST_N
68 APU_DBREQ_N

68,72 RST_CPU_N
46,68 PWR_SVID_PWRGD

24,44,46,72 PROCHOT_CPU_N

SVID

46 SVID_CLK_CPU
46 SVID_DATA_CPU
46 SVID_ALERT_CPU_N

46 VDDNB_SENSE
46 VCCCORE_SENSE

46 VSSCORE_SENSE

52 VDDP_S5_SENSE
52 VDDP_S0_SENSE

51 VDDIO_MEM_S3_SENSE

24 CPU_SMB_SDA_EC
24 CPU_SMB_SCL_EC

74 USB2_TCSS_AUX_CPU_P
74 USB2_TCSS_AUX_CPU_N
72 USB2_TPC_HPD

73 USB1_TCSS_AUX_CPU_P
73 USB1_TCSS_AUX_CPU_N
72 USB1_TPC_HPD

98 CPU_SMB_SDA
98 CPU_SMB_SCL

1D8V_S5
RN803 1 2 4 3 RST_CPU_N PWR_SVID_PWRGD
SRN4K7J-8-GP

HDT EVT stage要上

1D8V_S5
HDT PIN Pull High Resistor
ASM if HDT CONN is needs of use
RN804 1 2 3 4 8 7 6 5 APU_TDI APU_TCK APU_TRST_N APU_DBREQ_N
SRN1KJ-4-GP
HDT
R805 1 1KR2J-1-GP HDT APU_TMS

3D3V_S0
RN801 1 2 3 4 PROCHOT_CPU_N ALERT_N_CPU
SRN1KJ-7-GP
RN802 1 2 3 4 CPU_SMB_SCL CPU_SMB_SDA
SRN1KJ-7-GP
R803 1 1KR2J-1-GP THERMTRIP_N_CPU

C821 1 Do Not Stuff RST_CPU_N
C822 1 Do Not Stuff PWR_SVID_PWRGD

1D8V_S0
RN805 2 1 DY 4 CPU_SMB_SCL CPU_SMB_SDA
Do Not Stuff

RN801 change to 4 pin from 8 pin & add RN802
Add RN803 RSVD SIC/ SID 1D8V_S0 signal
Reserve 1.8v pull up at SIC & SID of CPU (Right now pull up 3.3v)_-1

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

APU1C
DISPLAY/SVI2/JTAG/TEST

eDP
eDP_TX_CPU_P0 D11 DP0_TXP0
eDP_TX_CPU_N0 B11 DP0_TXN0
eDP_TX_CPU_P1 C11 DP0_TXP1
eDP_TX_CPU_N1 A11 DP0_TXN1
D10 DP0_TXP2
B10 DP0_TXN2
D9 DP0_TXP3
B9 DP0_TXN3

HDMI
HDMI_DDI_TX_P0 G23 DP1_TXP0
HDMI_DDI_TX_N0 H23 DP1_TXN0
HDMI_DDI_TX_P1 F22 DP1_TXP1
HDMI_DDI_TX_N1 G22 DP1_TXN1
HDMI_DDI_TX_P2 G21 DP1_TXP2
HDMI_DDI_TX_N2 H21 DP1_TXN2
HDMI_DDI_TX_P3 F20 DP1_TXP3
HDMI_DDI_TX_N3 G20 DP1_TXN3

DP_BLON A22 PANEL_BLEN
DP_DIGON D23 EDP_VDD_EN
DP_VARY_BL C23 PANEL_BKLTCTL
DP0_AUXP D12 eDP_AUX_CPU_P
DP0_AUXN B12 eDP_AUX_CPU_N
DP0_HPD C12 EDP_HPD_CPU
DP1_AUXP J20 HDMI_SCL_CPU
DP1_AUXN K20 HDMI_SDA_CPU
DP1_HPD L21 HDMI_HPD_CPU
DP2_AUXP L19 USB1_TCSS_AUX_CPU_P
DP2_AUXN M19 USB1_TCSS_AUX_CPU_N
DP2_HPD M20 USB1_TPC_HPD
DP3_AUXP M14 USB2_TCSS_AUX_CPU_P
DP3_AUXN L14 USB2_TCSS_AUX_CPU_N
DP3_HPD L16 USB2_TPC_HPD
DP_STEREOSYNC B23 DP_STEREOSYNC_APU

eDP
R840 10KR2F-2-GP
R841 10KR2F-2-GP
HDMI
TYPEC USB1
TYPEC USB2

3D3V_S0
RN806 SRN2K2J-5-GP
HDMI_SCL_CPU
HDMI_SDA_CPU

TEST4 BB6 TEST4 1 TP808
TEST5 BD5 TEST5 1 TP807
TEST6 AG12
TEST14 G25 TEST14_APU 1 TP810
TEST15 K25 TEST15_APU 1 TP811
TEST16 F25 TEST16_APU 1 TP812
TEST17 F26 TEST17_APU 1 TP813
TEST31 H26 TEST31_APU 1 TP802
TEST41 AK9 TEST41 1 TP809
ANALOGIO_0 AK21
ANALOGIO_1 AG21

HDT
APU_TDI AP3 TDI
APU_TDO AU1 TDO
APU_TCK AR2 TCK
APU_TMS AU3 TMS
APU_TRST_N AR4 TRST_L
APU_DBREQ_N AT2 DBREQ_L

HDT
HDT CONN PIN#12 RST_CPU_N AW3 RESET#
HDT CONN PIN#10 PWR_SVID_PWRGD AW4 PWROK

CPU_SMB_SCL B22 SIC
CPU_SMB_SDA D22 SID
ALERT_N_CPU C22 ALERT_L
THERMTRIP_N_CPU AN9 THERMTRIP_L
PROCHOT_CPU_N B25 PROCHOT_L
an output signal as overtemperature condition

3D3V

SVID
SVID_CLK_CPU D25 SVC0
SVID_DATA_CPU C25 SVD0
SVID_ALERT_CPU_N A25 SVT0

FP6 REV 0.92
PART 3 OF 13
RENOIR-FP6-GP
ZZ.00CPU.421

SMU_ZVDD P3 0D75V_SMU_ZVDD R812 1 2 196R2F-GP
0D75V_S0

VDDP_S5_SENSE AK7 VDDP_S5_SENSE_APU R815 0R2-PT5-LILY-GP-U VDDP_S5_SENSE
VDDP_SENSE AK12 VDDP_S0_SENSE_APU R816 0R2-PT5-LILY-GP-U VDDP_S0_SENSE
VDDCR_SOC_SENSE J23 VDDNB_SENSE_APU R806 0R2-PT5-LILY-GP-U VDDNB_SENSE
VDDCR_SENSE K22 VCCCORE_SENSE_APU R807 0R2-PT5-LILY-GP-U VCCCORE_SENSE
VDDIO_MEM_S3_SENSE J21 VDDIO_MEM_S3_SENSE TP814
VSS_SENSE_A J22 VSS_SENSE_APU R809 0R2-PT5-LILY-GP-U VSSCORE_SENSE
VSS_SENSE_B AJ12 VSS_SENSEB TP801

C879 C889 C890 DY Do Not Stuff
if SI is not ok, suggest that install capacitor.
C890 ASM
for SVID Signal Quality test
Alert noise over spec 200mv_SC

VDDNB_SENSE R801 DY Do Not Stuff 1V_VDDCR_SOC
VCCCORE_SENSE R802 DY Do Not Stuff 1V_CPU_CORE
VSSCORE_SENSE R804 DY Do Not Stuff
VSS_SENSEB R817 DY Do Not Stuff

1D8V_S0
R837 1KR2F-L1-GP
DP_STEREOSYNC_APU
R808 DY Do Not Stuff

Check list: PD/CRB:PH

1D8V_S0 3D3V_S0
R810 DY Do Not Stuff
R811 0R402-DB-GP-U
3D3V_S0_SIC_SID
CPU_SMB_SDA Q808 CPU_SMB_SDA_EC
2N7002KDW-1-GP
75.27002.F7C
CPU_SMB_SCL_EC
CPU_SMB_SCL

L14 L15 LAN

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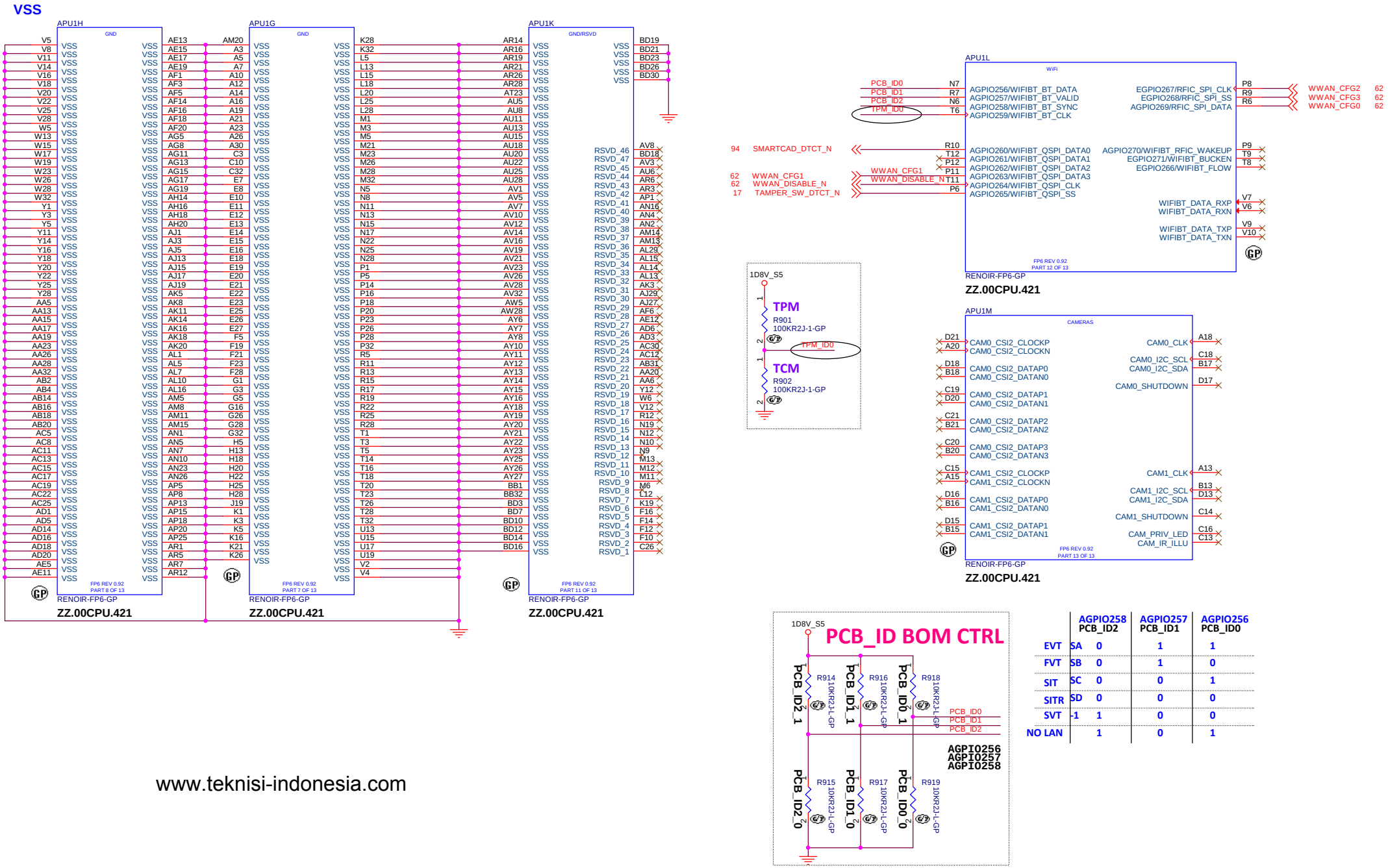
Title: CPU (DP/SVI/JTAG/TEST)
Size: A3 | Document Number: L14 L15 AMD | Rev: -1
Date: Wednesday, April 06, 2022 | Sheet 8 of 106



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	AGPIO258 PCB_ID2		AGPIO257 PCB_ID1	AGPIO256 PCB_ID0
EVT	SA	0	1	1
FVT	SB	0	1	0
SIT	SC	0	0	1
SITR	SD	0	0	0
SVT	-1	1	0	0
NO LAN		1	0	1

L14 L15 LAN

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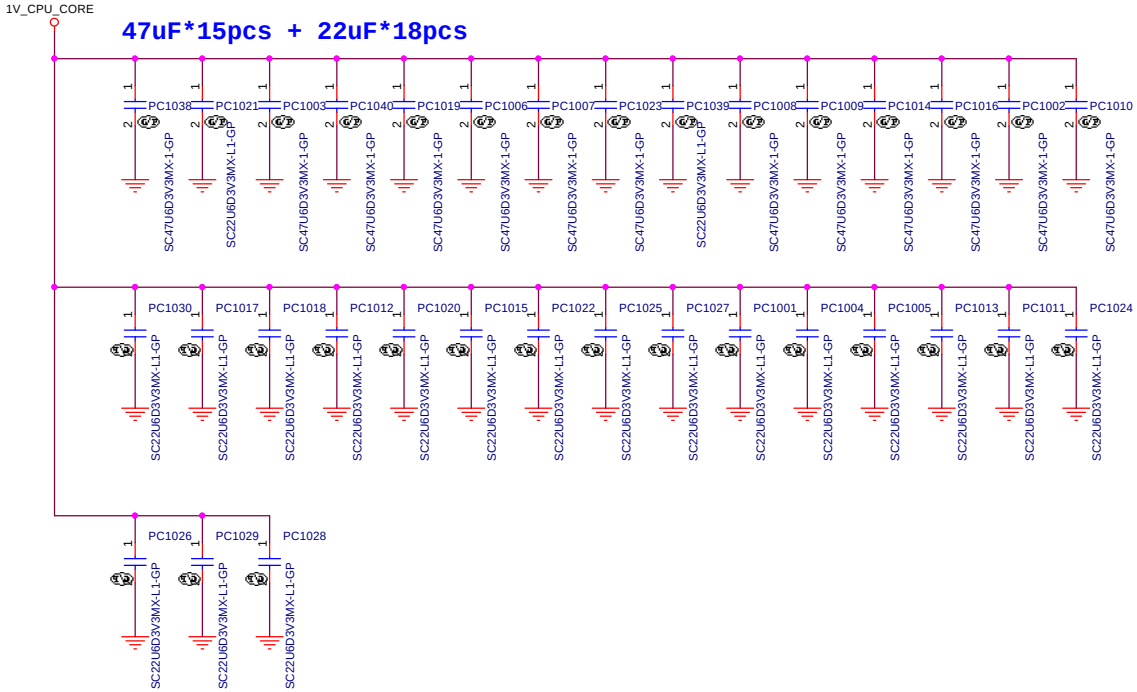
Title: CPU (VSS)

Size	Document Number	Rev
A3	L14 L15 AMD	-1

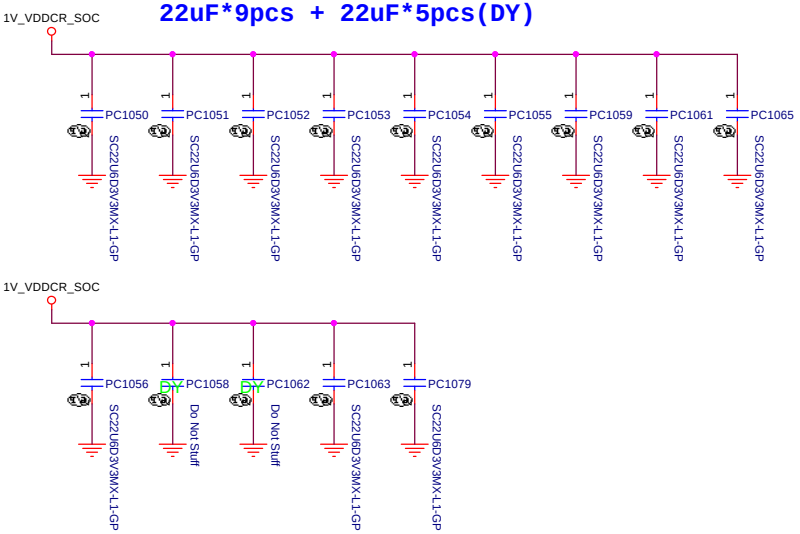
Date: Wednesday, April 06, 2022 Sheet 9 of 106

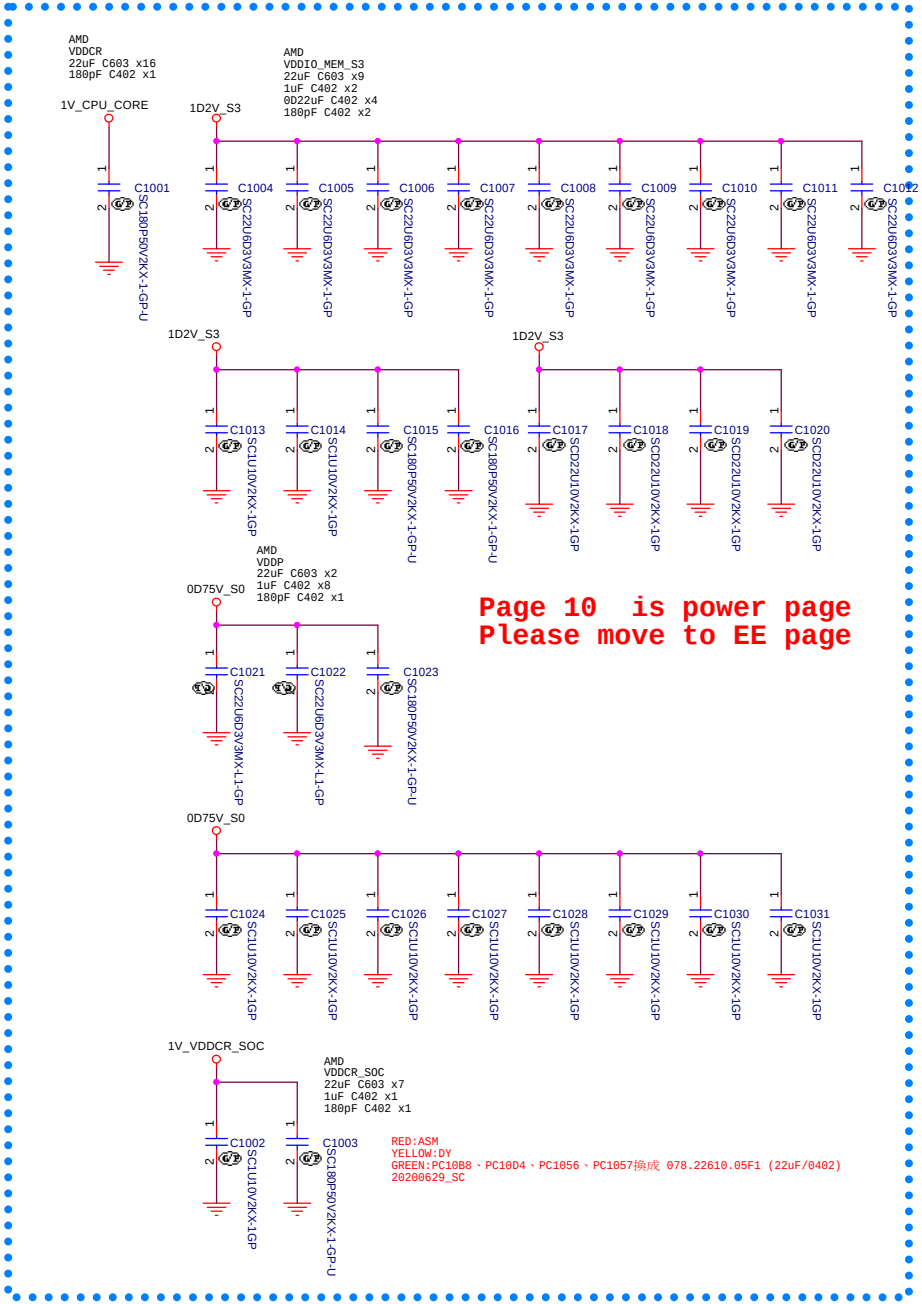
Main Func = CPU

1V_VDDCORE AMD_FP6_25W



1V_VDDCR_SOC





L14 L15 LAN

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Title	CPU(POWER CAP1)	
Size A3	Document Number L14 L15 AMD	Rev -1
Date: Wednesday, April 06, 2022	Sheet 10 of 106	

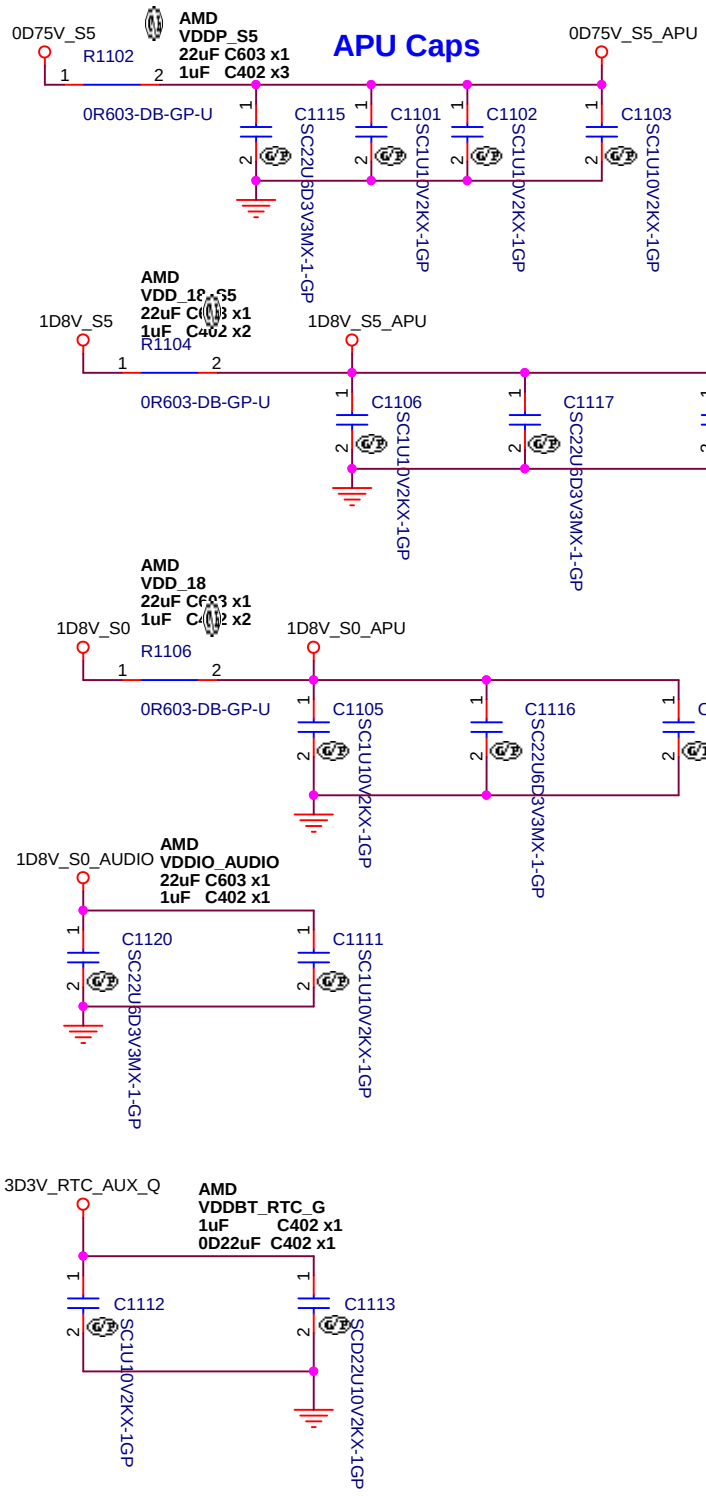

Table 110. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_SOC	VDDIO_MEM_S3[1, 2]	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTC_G
Value	Package Size / Material											
22 µF	0603 X5R	16BU	7BU	9BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 µF	0402 X5R	-	1BU	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU	1BU
0.22 µF	0402 X5R	-	-	4(split)	-	-	-	-	-	-	-	1BU
180 pF	0402 C0G NP0	1BU	1BU	1BU + 2(split)	1BU	-	-	-	-	-	-	-

L14 L15 LAN

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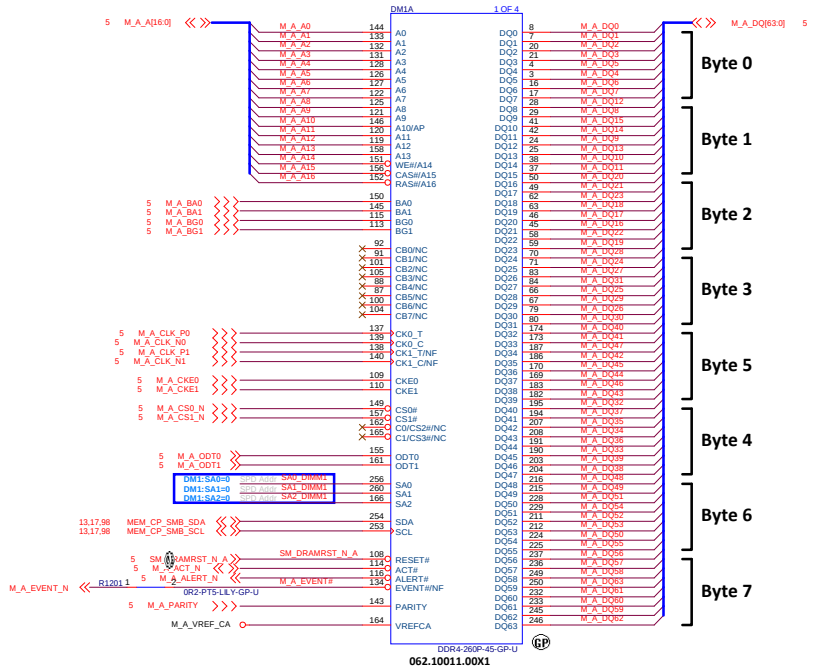
Title: **CPU (POWER CAP2)**

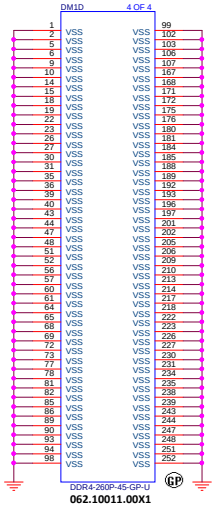
Size	Document Number	Rev
A4	**L14 L15 AMD**	-1

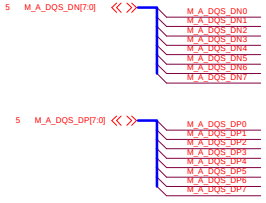
Date: Wednesday, April 06, 2022 Sheet 11 of 106

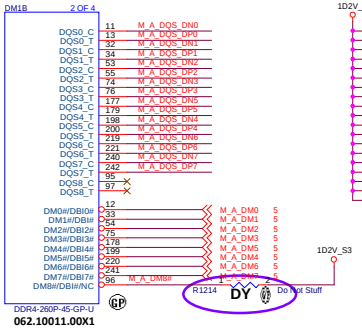
KL2_SIT_MB_W006

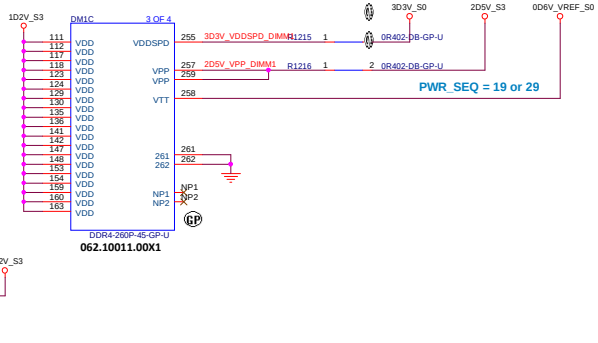
CHANNEL-A XMM1, A0, H=4.0mm



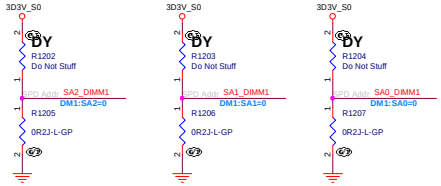








SPD Address of DM1



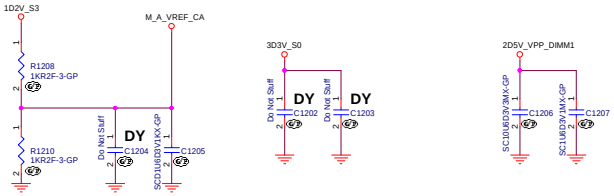
SPD SA2	0
SPD SA1	0
SPD SA0	0

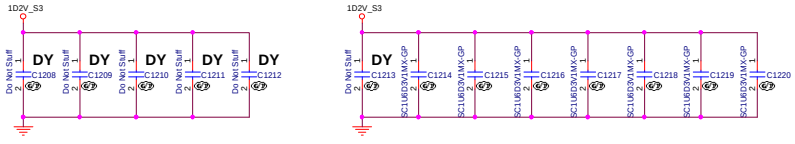
Note:
SA0 DM1 = 0, SA1_DM1 = 0
SA2 DM1 = 0
SO-DIMMA SPD Address is 0xA0

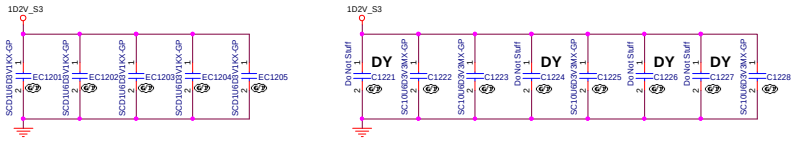
VREF CIRCUITRY

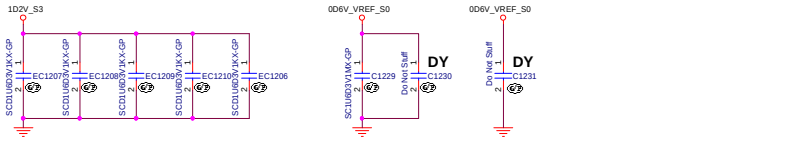
SA_DIMM_VREFDQ

Layout Note:
Place Close DM1









L14 L15 LAN

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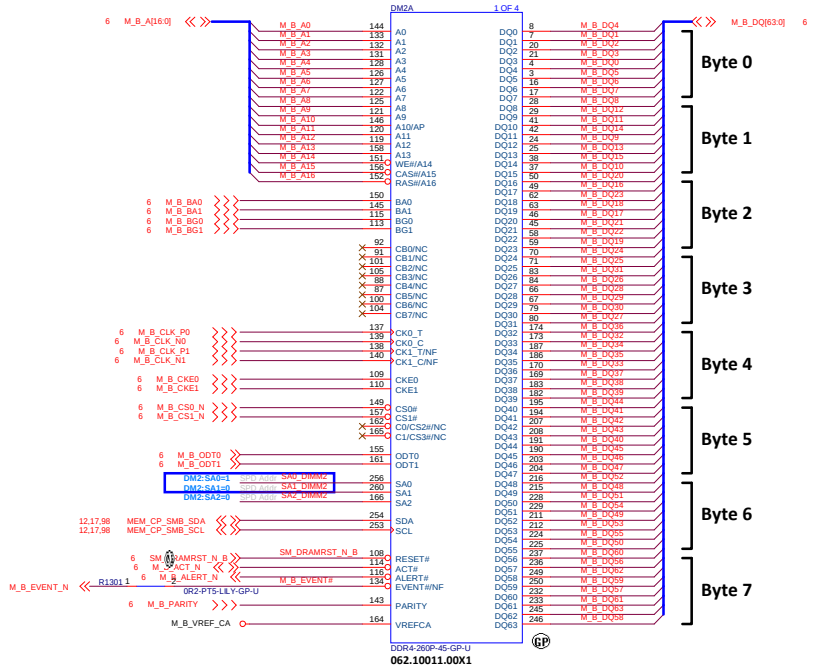
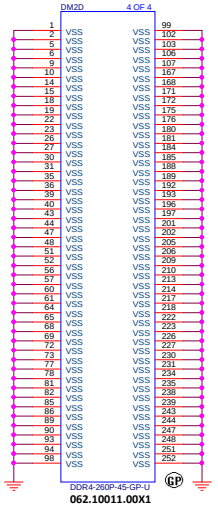
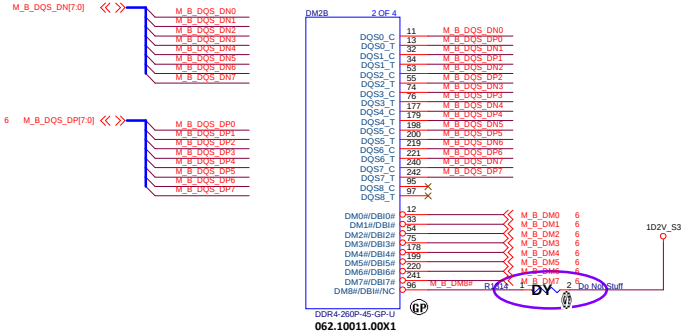
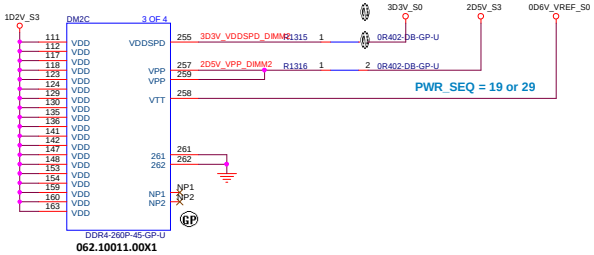
Title: DDR (DDR4-CHA SODIMM)		
Size: A2	Document Number: L14 L15 AMD	Rev: -1
Date: Wednesday, April 06, 2022	Sheet 12 of 106	

CHANNEL-B XMM1, A0, H=4.0mm

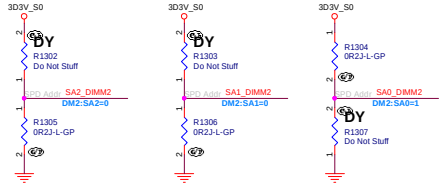








SPD Address of DM2



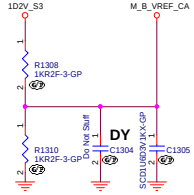
SPD SA2	0
SPD SA1	0
SPD SA0	1

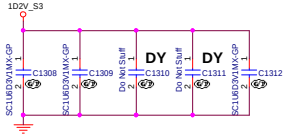
Note:
SA0 DM2 = 1, SA1_DM2 = 0
SA2 DM2 = 0
SO-DIMMB SPD Address is 0xA2

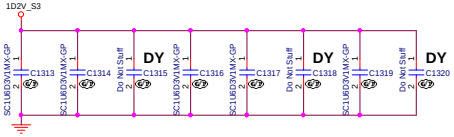
VREF CIRCUITRY

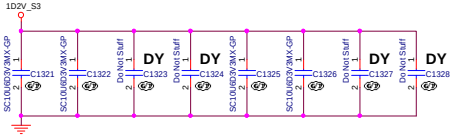
SA_DIMM_VREFDQ

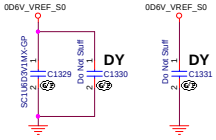
Layout Note:
Place Close DM2











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L14 L15 LAN

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Title: **DDR (DDR4-CHB SODIMM)**

Size	Document Number	Rev
A2	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 13 of 106

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L14 L15 LAN

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Title: ***DDR (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 14 of 106

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L14 L15 LAN

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Title: *FCH (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 15 of 106

CLK/SATA/USB/SPI/LPC

P_GPP CLK port	AMD	Device
0	GFX	NC
1	LAN	LAN
2	WWAN	CCD
3	PCIETBT	WWAN
4	PCIEDT	SD
5	SSD	SSD
6	WLAN	WLAN

LPCCLK1/EGPIO75
CLK_REQ5_L
If unused,
enable internal pull up or pull down by software.

GFX & GPP CLK, 85Ω
SATA & USB, 90Ω

WWAN
62 WWAN_CLK_CPU_P
62 WWAN_CLK_CPU_N
62 WWAN_CLKREQ_CPU_N

SSD
63 SSD_CLK_CPU_P
63 SSD_CLK_CPU_N
63 SSD_CLKREQ_CPU_N

WLAN
61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N

LAN
31 LAN_CLK_CPU_P
31 LAN_CLK_CPU_N
31 LAN_CLKREQ_CPU_N

CARD
66 CARD_CLK_CPU_P
66 CARD_CLK_CPU_N
66 CARD_CLKREQ_CPU_N

SPI
20,25,91 SPI_CLK_CPU
25,91 SPI_SO_CPU
25,91 SPI_SI_CPU
25 SPI_WP_CPU
25 SPI_HOLD_CPU
25 SPI_CS_CPU_N0

LPC
24 ECSMI_N_KBC
24,68,98 LPC_AD_CPU_P0
24,68,98 LPC_AD_CPU_P1
24,68,98 LPC_AD_CPU_P2
24,68,98 LPC_AD_CPU_P3
24,98 LPC_CLK_KBC
68 LPC_CLK_DBG
24,68 LPC_SERIRQ_CPU
24,68,98 LPC_FRAME_N_CPU
24,68,91 LPC_RST_N

91 PIRQA_N
24 ECSCI_N_KBC
24 KBRST_N
24,61 SUS_CLK_CPU
91 SPI_CS_CPU_N2
66 EC_SMI_APU
68 EGPIO141_RX
68 EGPIO143_TX
25 RTC_DET_N
63 M2_CARD_DET
65 TP4_RESET
90 NFC_DLREQ
66 CARD_DTCT

3D3V_S0
RN1601 1 2 4 3 SSD_CLKREQ_CPU_N WLAN_CLKREQ_CPU_N SRN10KJ-5-GP
RN1602 1 2 4 3 LAN_CLKREQ_CPU_N CARD_CLKREQ_CPU_N SRN10KJ-5-GP
R1601 1 10KR2J-3-GP WWAN_CLKREQ_CPU_N
R1620 1 10KR2J-3-GP LDRQ0_N
R1660 1 10KR2J-3-GP RTC_DET_N

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1D8V_S5
R1605 1 DY Do Not Stuff SUS_CLK_CPU
R1632 1 DY Do Not Stuff SPI_SI_CPU
R1658 1 10KR2J-3-GP M2_CARD_DET
M2_CARD_DET
0 -W/CARD ==>GND
1 -W/O CARD ==>PU

Follow FP6 CRB 20190424
R1635 1 2 0R2J-2-GP RSVD_71
R1636 1 2 0R2J-2-GP RSVD_70
C1603 1 DY Do Not Stuff LPC_RST_N
R1656 1 2 100KR2J-1-GP
EC1614 1 DY Do Not Stuff LPC_CLK_KBC
EC1615 1 DY Do Not Stuff LPC_CLK_DBG
C1616 1 DY Do Not Stuff LPC_SERIRQ_CPU

APU1E
CLK/LPC/EMMC/SD/SPI/eSPI/UART

LAN_CLKREQ_CPU_N AR13
WWAN_CLKREQ_CPU_N AP10
CARD_CLKREQ_CPU_N AR15
SSD_CLKREQ_CPU_N AT14
WLAN_CLKREQ_CPU_N AN11
AN13
AN15
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO92
CLK_REQ1_L/AGPIO115
CLK_REQ2_L/AGPIO116
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO131
CLK_REQ4_L/OSCIN/EGPIO132
CLK_REQ5_L/EGPIO120
CLK_REQ6_L/EGPIO121

LAN LAN_CLK_CPU_P AG4 LAN_CLK_CPU_N AG2
WWAN WWAN_CLK_CPU_P AF2 WWAN_CLK_CPU_N AF4
SD CARD CARD_CLK_CPU_P AH2 CARD_CLK_CPU_N AH4
SSD SSD_CLK_CPU_P AJ2 SSD_CLK_CPU_N AJ4
WLAN WLAN_CLK_CPU_P AF8 WLAN_CLK_CPU_N AF9

AF11 AF12 GPP_CLK0P GPP_CLK0N
AG3 AG1 GPP_CLK2P GPP_CLK2N
GPP_CLK1P GPP_CLK1N
GPP_CLK3P GPP_CLK3N
GPP_CLK4P GPP_CLK4N
GPP_CLK5P GPP_CLK5N
GPP_CLK6P/WIFIBT_CLKP
GPP_CLK6N/WIFIBT_CLKN

AK1 X48M_OSC
XTL_48M_X1_CPU BB3 X48M_X1
XTL_48M_X2_CPU BA5 X48M_X2
RSVD_71 AG10 RSVD_71
RSVD_70 AG9 RSVD_70
SUS_CLK_CPU AW10 RTCCLK
XTL_32K_X1_CPU AY1 X32K_X1
XTL_32K_X2_CPU AY4 X32K_X2

FP6 REV 0.92
PART 5 OF 13
RENOIR-FP6-GP

3D3V_S5
ECSMI_N_KBC R1606 1 10KR2J-3-GP

98 LPC_AD_CPU_P0_R
98 LPC_AD_CPU_P1_R
98 LPC_AD_CPU_P2_R
98 LPC_AD_CPU_P3_R
98 LPC_CLK_CPU_P0

pull high resistor is for eSPI LAR2 should be LPC

EGPIO70
LPC_PD_L/AGPIO21
LAD0/ESPI1_DATA0/EGPIO104
LAD1/ESPI1_DATA1/EGPIO105
LAD2/ESPI1_DATA2/EGPIO106
LAD3/ESPI1_DATA3/EGPIO107
LPCCLK0/EGPIO74
LPC_CLKRUN_L/AGPIO88
LPCCLK1/EGPIO75
SERIRQ/AGPIO87
LFRAME_L/EGPIO109
LPC_RST_L/AGPIO32
AGPIO68
LPC_PME_L/AGPIO22

AW14 CARD_DTCT
BB13 EC_SMI_APU R1602 1 0R0201-PAD-2-GP ECSMI_N_KBC
BA16 LPC_AD_CPU_P0_R R1626 1 10R1J-GP LPC_AD_CPU_P0
BA15 LPC_AD_CPU_P1_R R1627 1 10R1J-GP LPC_AD_CPU_P1
BC13 LPC_AD_CPU_P2_R R1628 1 10R1J-GP LPC_AD_CPU_P2
BB14 LPC_AD_CPU_P3_R R1629 1 10R1J-GP LPC_AD_CPU_P3
BB15 LPC_CLK_CPU_P0 R1608 1 22R1J-GP LPC_CLK_KBC
BD13 PIRQA_N
BA12 LPC_CLK_CPU_P1 R1609 1 22R1J-GP LPC_CLK_DBG
BC15 LPC_SERIRQ_CPU
BA13 LPC_FRAME_N_CPU
BC12 RST_N_APU R1612 1 33R1J-GP LPC_RST_N
AU12
AP4 ECSCI_N_KBC

to KBC

BA11 EGPIO67 1 TPAD14-OP-GP TP1605
BB11 EGPIO76 1 TPAD14-OP-GP TP1606

SPI_ROM_REQ/EGPIO67
SPI_ROM_GNT/EGPIO76
ESPI_RESET_L/KBRST_L/AGPIO129
ESPI_ALERT_L/LDRQ0_L/EGPIO108

AT15 KBRST_N
BC11 LDRQ0_N

SPI_CLK/ESPI_CLK
SPI_DI/ESPI_DATA
SPI_DO
SPI_WP_L/ESPI_DAT2
SPI_HOLD_L/ESPI_DAT3
SPI_CS1_L
SPI_CS2_L/ESPI_CS_L/AGPIO30
SPI_CS3_L/AGPIO31
SPI_TPM_CS_L/AGPIO29

BC10 SPI_CLK_CPU_R R1611 1 0R2J-2-GP SPI_CLK_CPU
BA10 SPI_SO_CPU_R R1613 1 33R2J-L1-GP SPI_SO_CPU
BB8 SPI_SI_CPU_R R1614 1 0R2J-2-GP SPI_SI_CPU
BA9 SPI_WP_CPU_R R1621 1 0R2J-2-GP SPI_WP_CPU
BC8 SPI_HOLD_CPU_R R1622 1 0R2J-2-GP SPI_HOLD_CPU
BD11 SPI_CS_CPU_N0_R R1607 1 0R2J-2-GP SPI_CS_CPU_N0
BC9
BB10 M2_CARD_DET
BD8 SPI_CS_CPU_N2

change TPM CS# pin from SPI_CS2_L/ESPI_CS_L/AGPIO30 to SPI_TPM_CS_L/AGPIO29 follow CRB_SC

DB_170410
Follow BIOS request for AMD LPC interface debug

EGPIO141/UART0_RXD
EGPIO143/UART0_TXD
EGPIO142/UART0_RTS_L/UART1_RXD
EGPIO140/UART0_CTS_L/UART1_TXD
AGPIO144/SHUTDOWN_L/UART0_INTR

BA17 EGPIO141_RX 1 TP1601
BC16 EGPIO143_TX 1 TP1602
BD15 NFC_DLREQ
BC17 RTC_DET_N
BB16 TP4_RESET_R R1659 1 33R1J-GP TP4_RESET

XTL_32K_X1_CPU R1649 1 33R2J-L1-GP 2 XTL_32K_X1
XTL_32K_X2_CPU R1650 1 33R2J-L1-GP 2 XTL_32K_X2
R1615 1 20MR2J-GP
X1602
XTAL-32D768KHZ-88-GP
082.30003.0191
C1601 SC15P50V2JN-2-GP
C1602 SC15P50V2JN-2-GP
78.15034.1FLLL is common part, but not in stock

Note:
Connected to 48-MHz Fundamental XTAL (±10 PPM) with a capacitor to GND as required by XTAL (typically 22 pF) and 1-M ohm 5% resistor to X48M_X2.
Connected to 48-MHz Fundamental XTAL (±10 PPM) with a capacitor to GND as required by XTAL (typically 22 pF) and 1-M ohm 5% resistor to X48M_X1.

XTL_48M_X1_CPU R1623 33R2J-L1-GP XTL_48M_X1
R1618 1MR2F-GP
X1601
C1612 SC10P50V2JN-4GP
XTAL-48MHZ-101-GP
082.30028.0491
XTL_48M_X2_CPU R1624 33R2J-L1-GP XTL_48M_X2
C1613 SC10P50V2JN-4GP

X1602	C1601	C1602	4ZA P/N	
EPSON 082.30003.0191	15pF	15pF	4ZA.0M501.0002	
NDK 082.30003.0221	15pF	15pF	4ZA.0M501.0003	NON COMMON
TXC 082.30003.0231	15pF	15pF	4ZA.0M501.0004	
TAITIEN 082.30003.0A11	15pF	15pF	4ZA.0M501.0005	
SEIKO 082.30003.0301	15pF	15pF	4ZA.0M501.0001	NON ECSL

X1602 32.768KHZ
EVT 082.30003.0A11/082.30003.0301/082.30003.0191
FVT 082.30003.0191/082.30003.0221/082.30003.0A11

X1601	C1612	C1613	ppm	
HARMONY 82.30026.371	10pF	10pF	20ppm	
TXC 082.30028.0091	10pF	10pF	20ppm	
TAITIEN 082.30028.0611	10pF	10pF	10ppm	NON ECSL/ NON COMMON
HOSONIC 082.30028.0511			10ppm	NON ECSL/ NON COMMON

X1601 48MHZ
EVT 082.30028.0611/82.30026.371/082.30028.0091
FVT 82.30026.371/082.30028.0091/082.30028.0611

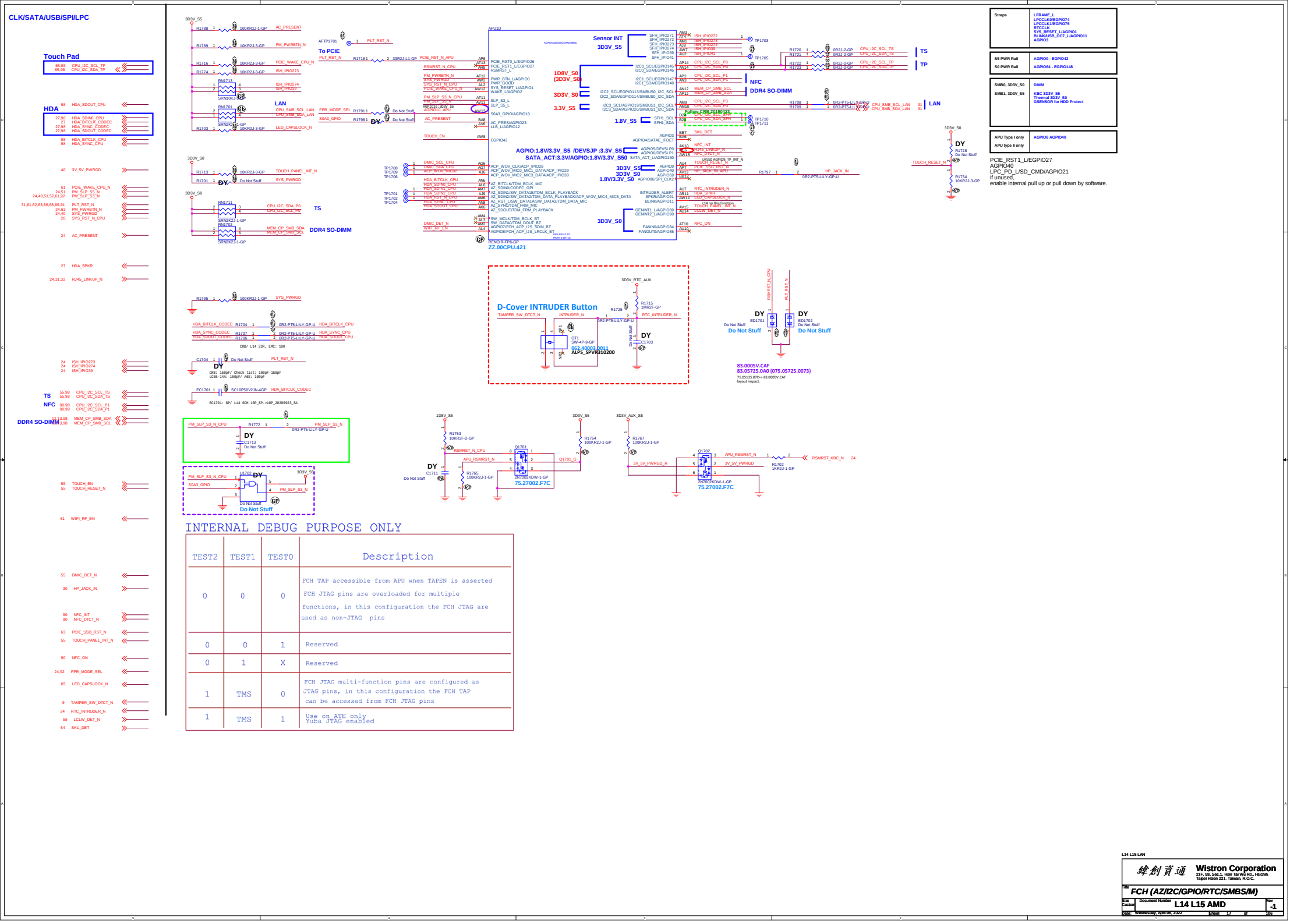
L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **FCH (CLK/LPC/SPI/EMMC/SD/UA)**

Size: A3 | Document Number: **L14 L15 AMD** | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 16 of 106



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

Straps	LFRAME_L LPCCLK0/EGPIO74 LPCCLK1/EGPIO75 RTCCLK SYS_RESET_L/AGPIO1 BLINK/USB_OC7_L/AGPIO11 AGPIO3
S5 PWR Rail	AGPIO0 - EGPIO42
S0 PWR Rail	AGPIO64 - EGPIO148
SMB0, 3D3V_S0	DIMM
SMB1, 3D3V_S5	KBC 3D3V_S5 Thermal 3D3V_S0 GSENSOR for HDD Protect
APU Type I only	AGPIO8 AGPIO40
APU type II only	

L14 L15 LAN

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (AZ/I2C/GPIO/RTC/SMBS/M)

Size: Custom | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 17 of 108

USB3.0 Port3

36 USB3_USB31_RX_N
36 USB3_USB31_RX_P
36 USB3_USB31_TX_N
36 USB3_USB31_TX_P

35 USB3_USB20_N
35 USB3_USB20_P

USB3.0 Port4

66 USB4_USB31_RX_N
66 USB4_USB31_RX_P
66 USB4_USB31_TX_N
66 USB4_USB31_TX_P

66 USB4_USB20_N
66 USB4_USB20_P

BT

61 BT_USB20_N
61 BT_USB20_P

HUB

38 HUB_USB20_P
38 HUB_USB20_N

WWAN

62 WWAN_USB20_P
62 WWAN_USB20_N

Type-C USB20

73 USB1_USB20_N
73 USB1_USB20_P

Type-C DK1

73 USB1_TCSS_TX_P0
73 USB1_TCSS_TX_N0
73 USB1_TCSS_RX_P0
73 USB1_TCSS_RX_N0

73 USB1_TCSS_TX_P1
73 USB1_TCSS_TX_N1
73 USB1_TCSS_RX_P1
73 USB1_TCSS_RX_N1

Type-C 2 USB20

74 USB2_USB20_N
74 USB2_USB20_P

Type-C 2

74 USB2_TCSS_TX_P0
74 USB2_TCSS_TX_N0
74 USB2_TCSS_RX_P0
74 USB2_TCSS_RX_N0

74 USB2_TCSS_TX_P1
74 USB2_TCSS_TX_N1
74 USB2_TCSS_RX_P1
74 USB2_TCSS_RX_N1

66 USB_OC1_N
35,72 USB_OC0_N

72 CPU_I2C_SCL_PD
72 CPU_I2C_SDA_PD

FP

92 FP_USB20_P
92 FP_USB20_N

65 PAD_INT_N
62 WWAN_PEWAKE_N

Type-C port1
USB2.0 Port3
BT
FP
Type-C 2 port2
USB2.0 Port4
HUB
WWAN

USB1_USB20_P AC6
USB1_USB20_N AC7
USB3_USB20_P AA8
USB3_USB20_N AA9
BT_USB20_P Y10
BT_USB20_N Y9
FP_USB20_P Y7
FP_USB20_N Y6
USB2_USB20_P AC9
USB2_USB20_N AC10
USB4_USB20_P AA11
USB4_USB20_N AA12
HUB_USB20_P W8
HUB_USB20_N W9
WWAN_USB20_P W11
WWAN_USB20_N W12

CPU_I2C_SCL_TYPEC AL9
CPU_I2C_SDA_TYPEC AL8

USB_OC0_N AE9
WWAN_PEWAKE_N AE10
PAD_INT_N AE6
USB_OC1_N AE7

APU1J

USBC0_DP/USB0_DP
USBC0_DN/USB0_DN
USB1_DP
USB1_DN
USB2_DP
USB2_DN
USB3_DP
USB3_DN
USBC4_DP/USB4_DP
USBC4_DN/USB4_DN
USB5_DP
USB5_DN
USB6_DP
USB6_DN
USB7_DP
USB7_DN
USBC_I2C_SCL
USBC_I2C_SDA
USB_OC0_L/AGPIO16
USB_OC1_L/AGPIO17
USB_OC2_L/AGPIO18
USB_OC3_L/AGPIO24

USBC0_TX1P/USB0_TXP/DP2_TXP2
USBC0_TX1N/USB0_TXN/DP2_TXN2
USBC0_RX1P/USB0_RXP/DP2_TXP3
USBC0_RX1N/USB0_RXN/DP2_TXN3
USBC0_TX2P/DP2_TXP1
USBC0_TX2N/DP2_TXN1
USBC0_RX2P/DP2_TXP0
USBC0_RX2N/DP2_TXN0
USB1_TXP
USB1_TXN
USB1_RXP
USB1_RXN
USBC4_TX1P/USB4_TXP/DP3_TXP2
USBC4_TX1N/USB4_TXN/DP3_TXN2
USBC4_RX1P/USB4_RXP/DP3_TXP3
USBC4_RX1N/USB4_RXN/DP3_TXN3
USBC4_TX2P/DP3_TXP1
USBC4_TX2N/DP3_TXN1
USBC4_RX2P/DP3_TXP0
USBC4_RX2N/DP3_TXN0
USB5_TXP
USB5_TXN
USB5_RXP
USB5_RXN

FP6 REV 0.92
PART 10 OF 13

RENOIR-FP6-GP

1.8V_S5

AA1 USB1_TCSS_TX_P0
AA3 USB1_TCSS_TX_N0
AA2 USB1_TCSS_RX_P0
AA4 USB1_TCSS_RX_N0
AC2 USB1_TCSS_TX_P1
AC4 USB1_TCSS_TX_N1
AC1 USB1_TCSS_RX_P1
AC3 USB1_TCSS_RX_N1
AE1 USB3_USB31_TX_P
AE3 USB3_USB31_TX_N
AD8 USB3_USB31_RX_P
AD9 USB3_USB31_RX_N

Type C USB3.1 Gen2 + USB2.0 + DP
Type-C port1
USB3.0 Port3

V3 USB2_TCSS_TX_P0
V1 USB2_TCSS_TX_N0
U4 USB2_TCSS_RX_P0
U2 USB2_TCSS_RX_N0
W2 USB2_TCSS_TX_P1
W4 USB2_TCSS_TX_N1
W1 USB2_TCSS_RX_P1
W3 USB2_TCSS_RX_N1
AD2 USB4_USB31_TX_P
AD4 USB4_USB31_TX_N
AD12 USB4_USB31_RX_P
AD11 USB4_USB31_RX_N

Type C USB3.1 Gen1 + USB2.0 + DP
Type-C 2 port2
USB3.0 Port4

3D3V_S5
RN1802
1 2 4 3
USB_OC1_N
USB_OC0_N
SRN10KJ-3GP

ZZ.00CPU.421

AGPIO13/USB_OC5_L
If unused,
enable internal pull up or pull down by software.

1D8V_S5
R1803
0R402-DB-GP-U
C1801
SCD1U16V2KX-3GP
1D8V_S5_PD
Q1801
CPU_I2C_SCL_PD
CPU_I2C_SCL_TYPEC
CPU_I2C_SDA_PD
CPU_I2C_SDA_TYPEC
PJT138KA-GP
075.00138.0A7C

98 CPU_I2C_SCL_TYPEC
98 CPU_I2C_SDA_TYPEC

1D8V_S5
RN1803
CPU_I2C_SCL_TYPEC
CPU_I2C_SDA_TYPEC
SRN4K7J-8-GP

L14 L15 LAN

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FCH (USB/CAMERA/RSVD)
Size: A3
Document Number: L14 L15 AMD
Rev: -1
Date: Wednesday, April 06, 2022
Sheet 18 of 106

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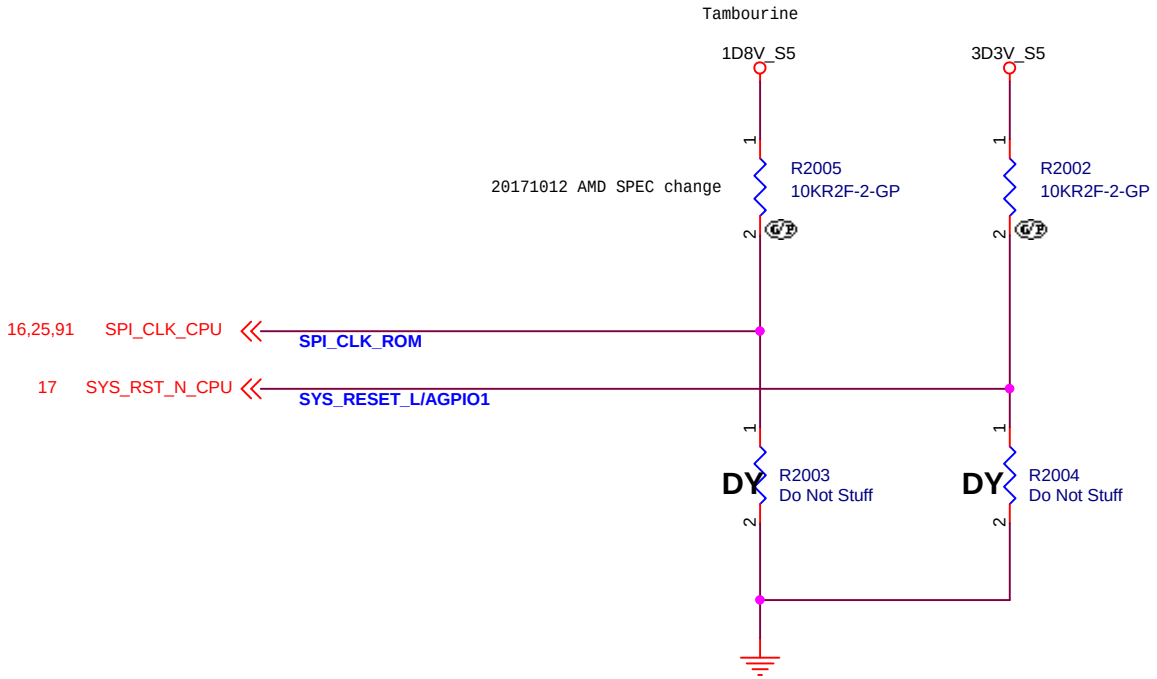
L14 L15 LAN

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***FCH (RSVD)***		
Size: A4	Document Number: **L14 L15 AMD**	Rev: **-1**
Date: Wednesday, April 06, 2022	Sheet 19 of 106	

STRAP PINS



	PIN SPI_CLK NET SPI_CLK_ROM	PIN SYS_RESET_L//AGPIO1 NET SYS_RST#_CPU
PULL HIGH	Configured for internal clock-generator 10kΩ(± 5%) pull-up resistor to VDD_18 (DEFAULT)	Normal powerup / reset timing 10KΩ(± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)
PULL LOW	Reserved	Reserved

L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***FCH (STRAP)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	-1

Date: Wednesday, April 06, 2022 Sheet 20 of 106

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L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *FCH (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 21 of 106

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L14 L15 LAN

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *FCH (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 22 of 106

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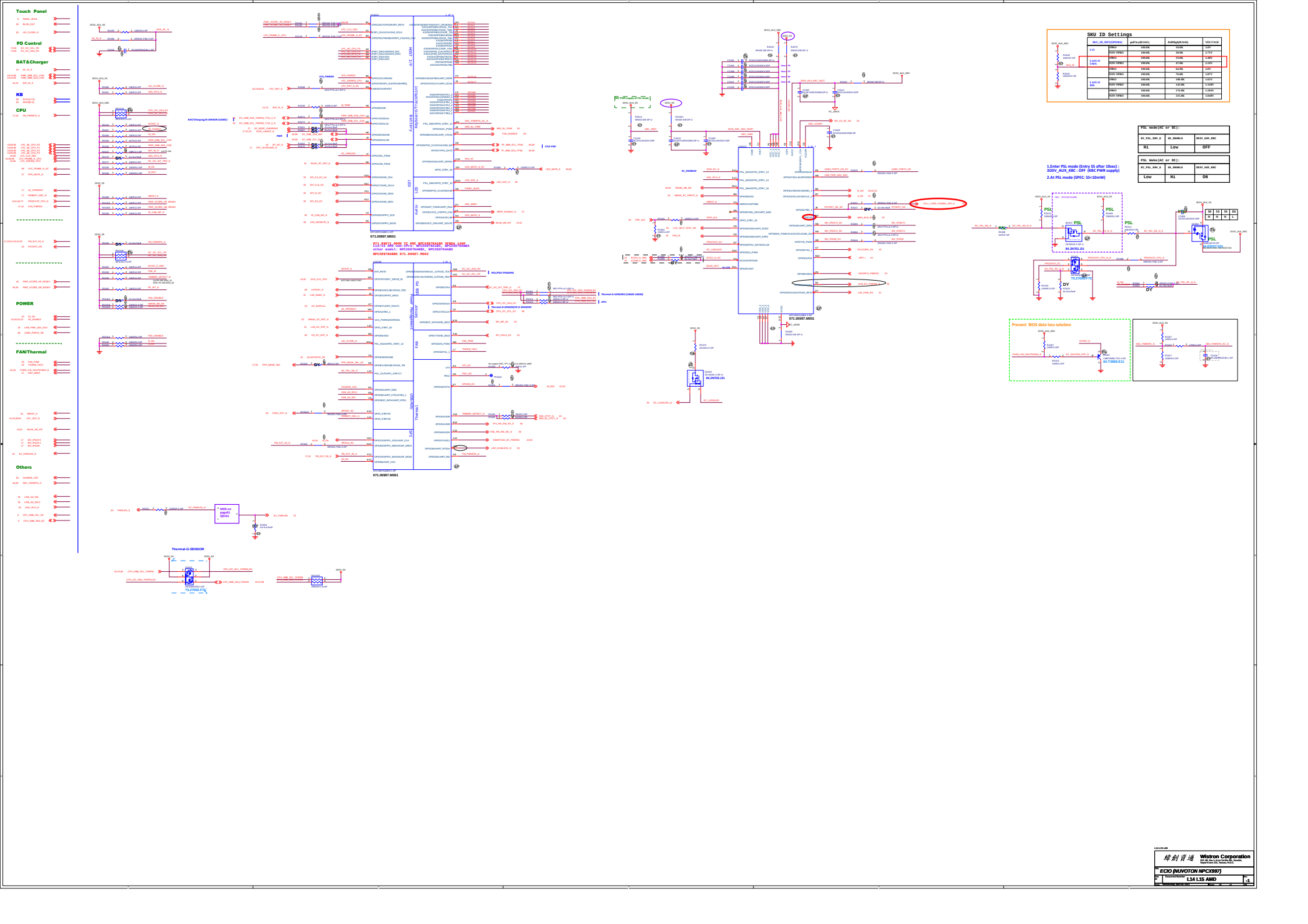
L14 L15 LAN

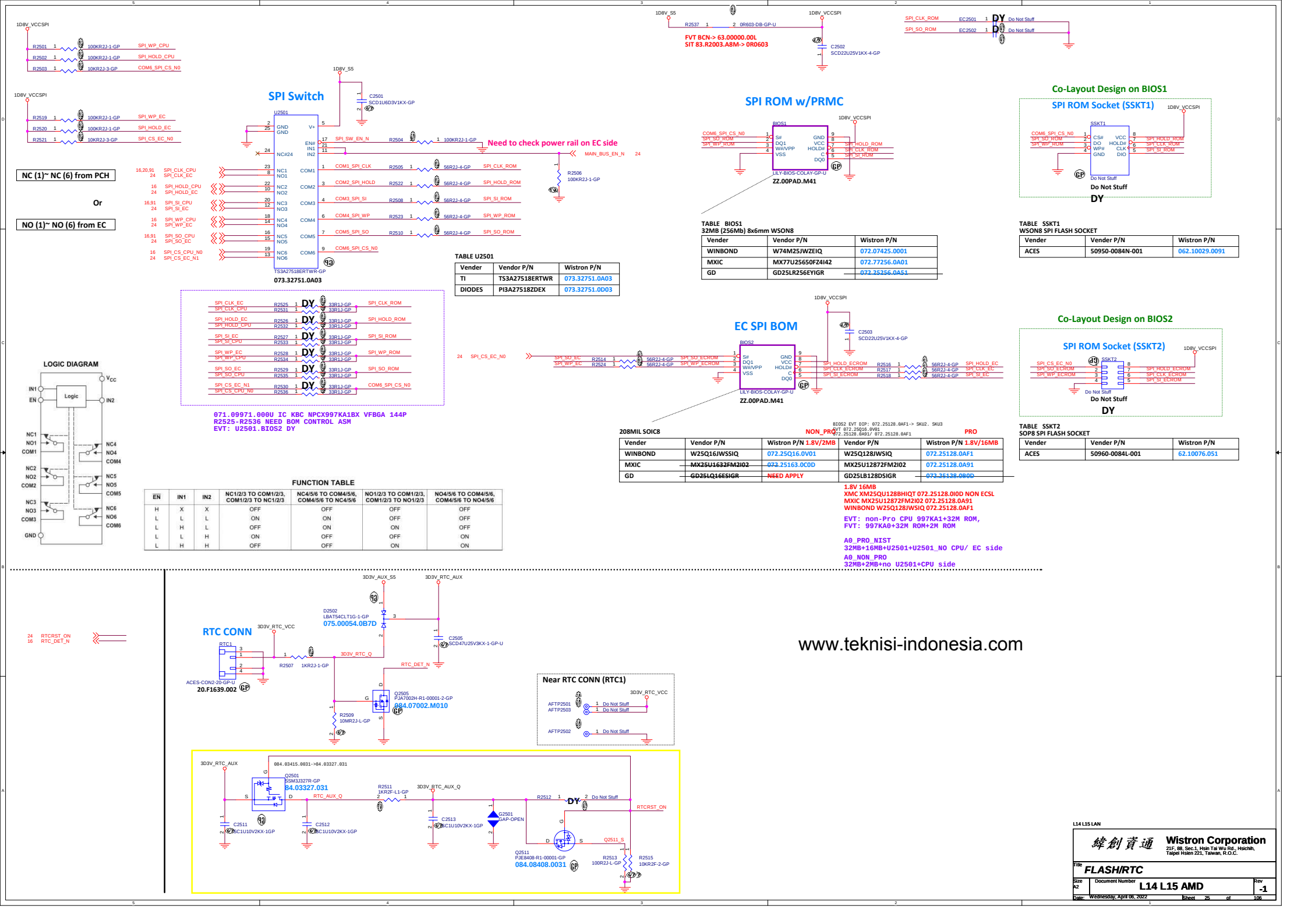
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *FCH (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 23 of 106


Touch Panel
PD Control
BAT&Charger
KB
CPU
FAN/Thermal
POWER
Others
SKU ID Settings
PSL mode(AC or DC):
PSL Wake(AC or DC):
1.Enter PSL mode (Entry S5 after 10sec) : 3V3V_AUX_KBC : OFF (KBC PWR supply)
2.At PSL mode (SPEC: S5<10mW)
Prevent BIOS data loss solution
Thermal-G-SENSOR
ECIO (NUVOTON NPCX997)
L34 L35 AMD
Wistron Corporation


1D8V_VCCSPI
R2501 100KR2J-1-GP SPI_WP_CPU
R2502 100KR2J-1-GP SPI_HOLD_CPU
R2503 10KR2J-3-GP COM6_SPI_CS_N0
R2519 100KR2J-1-GP SPI_WP_EC
R2520 100KR2J-1-GP SPI_HOLD_EC
R2521 10KR2J-3-GP SPI_CS_EC_N0
NC (1)~ NC (6) from PCH
Or
NO (1)~ NO (6) from EC
SPI Switch
U2501
TS3A27518ERTWR-GP
073.32751.0A03
1D8V_S5
C2501 SCD1U6D3V1KX-GP
SPI_SW_EN_N
R2504 100KR2J-1-GP
Need to check power rail on EC side
MAIN_BUS_EN_N
R2506 100KR2J-1-GP
SPI_CLK_CPU
SPI_CLK_EC
SPI_HOLD_CPU
SPI_HOLD_EC
SPI_SI_CPU
SPI_SI_EC
SPI_WP_CPU
SPI_WP_EC
SPI_SO_CPU
SPI_SO_EC
SPI_CS_CPU_N0
SPI_CS_EC_N1
COM1_SPI_CLK
COM2_SPI_HOLD
COM3_SPI_SI
COM4_SPI_WP
COM5_SPI_SO
COM6_SPI_CS_N0
56R2J-4-GP
SPI_CLK_ROM
SPI_HOLD_ROM
SPI_SI_ROM
SPI_WP_ROM
SPI_SO_ROM
TABLE U2501
Vender | Vendor P/N | Wistron P/N
TI | TS3A27518ERTWR | 073.32751.0A03
DIODES | PI3A27518ZDEX | 073.32751.0D03
DY
33R1J-GP
071.09971.000U IC KBC NPCX997KA1BX VFBGA 144P
R2525-R2536 NEED BOM CONTROL ASM
EVT: U2501.BIOS2 DY
LOGIC DIAGRAM
Logic
FUNCTION TABLE
EN | IN1 | IN2 | NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3 | NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6 | NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3 | NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6
H X X OFF OFF OFF OFF
L L L ON ON OFF OFF
L H L OFF ON ON OFF
L L H ON OFF OFF ON
L H H OFF OFF ON ON
SPI ROM w/PRMC
BIOS1
LILY-BIOS-COLAY-GP-U
ZZ.00PAD.M41
TABLE BIOS1
32MB (256Mb) 8x6mm WSON8
Vender | Vendor P/N | Wistron P/N
WINBOND | W74M25JWZEIQ | 072.07425.0001
MXIC | MX77U25650FZ4I42 | 072.77256.0A01
GD | GD25LR256EYIGR | 072.25256.0A51
EC SPI BOM
BIOS2
208MIL SOIC8
NON_PRO
PRO
BIOS2 EVT DIP: 072.25128.0AF1-> SKU2. SKU3
EVT 072.25Q16.0V01
072.25128.0A91/ 072.25128.0AF1
Vender | Vendor P/N | Wistron P/N 1.8V/2MB | Vendor P/N | Wistron P/N 1.8V/16MB
WINBOND | W25Q16JWSSIQ | 072.25Q16.0V01 | W25Q128JWSIQ | 072.25128.0AF1
MXIC | MX25U1632FM2I02 | 072.25163.0C0D | MX25U12872FM2I02 | 072.25128.0A91
GD | GD25LQ16ESIGR | NEED APPLY | GD25LB128DSIGR | 072.25128.080D
1.8V 16MB
XMC XM25QU128BHIQT 072.25128.0I0D NON ECSL
MXIC MX25U12872FM2I02 072.25128.0A91
WINBOND W25Q128JWSIQ 072.25128.0AF1
EVT: non-Pro CPU 997KA1+32M ROM,
FVT: 997KA0+32M ROM+2M ROM
A0_PRO_NIST
32MB+16MB+U2501+U2501_NO CPU/ EC side
A0_NON_PRO
32MB+2MB+no U2501+CPU side
FVT BCN-> 63.00000.00L
SIT 83.R2003.A8M-> 0R0603
R2537 0R603-DB-GP-U
C2502 SCD22U25V1KX-4-GP
C2503 SCD22U25V1KX-4-GP
EC2501
EC2502
Do Not Stuff
Co-Layout Design on BIOS1
SPI ROM Socket (SSKT1)
SSKT1
Do Not Stuff
DY
TABLE SSKT1
WSON8 SPI FLASH SOCKET
Vender | Vender P/N | Wistron P/N
ACES | 50950-0084N-001 | 062.10029.0091
Co-Layout Design on BIOS2
SPI ROM Socket (SSKT2)
SSKT2
TABLE SSKT2
SOP8 SPI FLASH SOCKET
Vender | Vender P/N | Wistron P/N
ACES | 50960-0084L-001 | 62.10076.051
RTCRST_ON
RTC_DET_N
RTC CONN
RTC1
ACES-CON2-20-GP-U
20.F1639.002
3D3V_RTC_VCC
3D3V_AUX_S5
3D3V_RTC_AUX
D2502 LBAT54CLT1G-1-GP
075.00054.0B7D
C2505 SCD47U25V3KX-1-GP-U
R2507 1KR2J-1-GP
3D3V_RTC_Q
Q2505 PJA7002H-R1-00001-2-GP
084.07002.M010
R2509 10MR2J-L-GP
Near RTC CONN (RTC1)
AFTP2501
AFTP2502
AFTP2503
Do Not Stuff
Q2501 SSM3J327R-GP
084.03327.031
084.03415.0031->084.03327.031
RTC_AUX_Q
R2511 1KR2F-L1-GP
3D3V_RTC_AUX_Q
C2511 SC1U10V2KX-1GP
C2512 SC1U10V2KX-1GP
C2513 SC1U10V2KX-1GP
G2501 GAP-OPEN
R2512
Q2511_S
Q2511 PJE8408-R1-00001-GP
084.08408.0031
R2513 100R2J-L-GP
R2515 10KR2F-2-GP
www.teknisi-indonesia.com
L14 L15 LAN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title FLASH/RTC
Size A2
Document Number L14 L15 AMD
Rev -1
Date: Wednesday, April 06, 2022
Sheet 25 of 106

Thermal Sensor

Sensor	Target
U2601	Charger
U2603	CPU

Close to PL4401(Charger)

Ch2

Q2602 LMBT3904LT1G-GP 84.T3904.H11

C2608 DY Do Not Stuff

SC2K2P50V2KX-L-GP C2615

THERM_DXP_7718_2

THERM_DXN_7718_2

Close to CPU (APU1)

2200p close to Thermal Sensor chip

Ch1

T8

Q2601 LMBT3904LT1G-GP 84.T3904.H11

C2609 DY Do Not Stuff

SC2K2P50V2KX-L-GP C2604

THERM_DXP_7718

THERM_DXN_7718

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

ALERT# /T_CRIT# Pull-up Resistor v.s. Alert temperature (℃)

NCT7717U Table:

R2630	
2.0K	75
7.5K	90
10.5K	100
14.0K	105
18.7K	110

NCT7718W Table:

R2619 \ R2621 \(R1633/ (R1632)	2.0K	7.5K	10.5K	14.0K	18.7K
2.0K	77	87	97	107	117
7.5K	79	89	99	109	119
10.5K	81	91	101	111	121
14.0K	83	93	103	113	123
18.7K	85	95	105	115	125

3D3V_S0

R2620 10K5R2F-GP THERM_SYS_SHDN_N

R2633 DY Do Not Stuff NTC7718_CRIT_N

R2619 10K5R2F-GP NTC7718_2_CRIT_N

R2632 DY Do Not Stuff THERM_ALERT_N_7718

R2621 18K7R2F-GP THERM_ALERT_N_7718_2

R2630 14KR2F-GP THERM_ALERT_N_GMT

ALERT# point hardware power-on setting

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

PULL-UP RESISTOR		TEMPERATURE (°C)
ALERT	2kΩ	75
	7.5kΩ	90
	10.5kΩ	100
	14kΩ	105
	18.7kΩ	110

TABLET

ID	Target	Function
RT2601		
RT2602		
RT2603		
RT2605		
RT2606		
RT2607		
RT2608		

3D3V_S0

C2614 SC1U10V2KX-1GP

C2613 SCD1U6D3V1KX-GP

R2626 0R402-DB-GP-U

U2601 NCT7718W-GP

VDD D+ D- T_CRIT# SCL SDA ALERT# GND

THERM_SYS_SHDN_N D2603 DY Do Not Stuff

3D3V_S0_THERM_7718_2 THERM_DXP_7718_2 THERM_DXN_7718_2 NTC7718_2_CRIT_N

RN2602 SRN2K2J-5-GP

R2622 R2623 0R2-PT5-LILY-GP-U

THERM_SMB_SCL_7718_2 THERM_SMB_SDA_7718_2 THERM_ALERT_N_7718_2

EC_SMB_SCL_THERM_7718_2 EC_SMB_SDA_THERM_7718_2

74.07718.0B9

Close to Charger

98 THERM_SMB_SCL_7718_2

98 THERM_SMB_SDA_7718_2

3D3V_S0

Q2607 2N7002KDW-1-GP 75.27002.F7C

EC_SMB_SCL_THERM_7718_2 EC_SMB_SCL_THERM_7718_2_R 24

24 EC_SMB_SDA_THERM_7718_2_R EC_SMB_SDA_THERM_7718_2

FAN Controller

NCT7718W 's maximum power consumption can be xxx mA (TBD)

Layout NOTE:
VDD trace width: 20 mil less

3D3V_S0

C2605 SC1U10V2KX-1GP

C2603 SCD1U6D3V1KX-GP

R2601 0R402-DB-GP-U

U2603 G781-1P8F-GP

VCC DXP DXN THERM# SMBCLK SMBDATA ALERT# GND

THERM_SYS_SHDN_N D2604 DY Do Not Stuff

3D3V_S0_THERM_7718 THERM_DXP_7718 THERM_DXN_7718 NTC7718_CRIT_N

CPU_SMB_SCL_THERM_7718 CPU_SMB_SDA_THERM_7718 THERM_ALERT_N_7718

R2624 R2625 33R2J-L1-GP

CPU_SMB_SCL_THERM CPU_SMB_SDA_THERM 24,70,98

74.00781.C89

Close to CPU

98 CPU_SMB_SCL_THERM_7718

98 CPU_SMB_SDA_THERM_7718

3D3V_S0

C2616 SC1U10V2KX-1GP

C2617 SCD1U6D3V1KX-GP

R2602 0R402-DB-GP-U

U2604 G753T11U-GP

SMBDATA VS+ SMBCLK GND ALERT#

3D3V_S0_THERM_GMT

CPU_SMB_SDA_THERM_GMT R2638 10KR2J-2-GP-U CPU_SMB_SDA_THERM

CPU_SMB_SCL_THERM_GMT R2637 10KR2J-2-GP-U CPU_SMB_SCL_THERM

THERM_ALERT_N_GMT D2601 Do Not Stuff THERM_SYS_SHDN_N

DY

074.75311.007F

Close to Charger

3D3V_S0

RN2601 SRN10KJ-5-GP

THERM_TACH FAN_PWM FAN_ID

24 THERM_TACH 24 FAN_PWM 24 FAN_ID

83.R5003.H8H

D2602 D2614 RB551V30-GP 0R2-PT5-LILY-GP-U

5V_S0

0R by Project Team requested

D1 DY Do Not Stuff C2612

R2605 0R0603-DB-GP-U

R2606 10KR2J-3-GP

5V_S0_FAN FAN_TACH FAN_PWM_C

FAN CONN

FAN1 ACES-CON6-91-GP 020.F1803.M001

DY Do Not Stuff EC2601

DY Do Not Stuff EC2602

Near FAN CONN (FAN1)

AFTP2601	1 Do Not Stuff	5V_S0_FAN
AFTP2602	1 Do Not Stuff	FAN_TACH
AFTP2603	1 Do Not Stuff	FAN_PWM_C
AFTP2604	1 Do Not Stuff	FAN_ID
AFTP2605	1 Do Not Stuff	

24,40 PURE_HW_SHUTDOWN_N

Q2604 T2N7002BK-2-GP 084.27002.0L31

DY R2610 Do Not Stuff

DY C2607 Do Not Stuff

THERM_SYS_SHDN_N

R2608 10KR2J-3-GP

PWR_VCORE_NB_READY 24,46

3D3V_S0

PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low

PTC-5402-2-GP RT2607 RT2608 RT_5 RT_4

PTC-5402-2-GP RT2605 RT2606 RT_3

PTC-5402-2-GP RT2603 RT_2 RT_1

PTC-5402-2-GP RT2601 RT2602 RT_0

SCD1U6D3V1KX-GP C2611

5V_S5

R2617 6K81R2F-L-GP

5V *100K/(100K+40K) = 3.57V

R2616 40K2R2F-GP

R2618 100KR2F-L1-GP

RT_COMP+ RT_COMP-

SCD1U6D3V1KX-GP C2610

U2602 LMV331IDCKR-4-GP 74.00331.A2F

RT_COMP_OUT

3D3V_AUX_S5

R2613 100KR2J-1-GP

R2615 RT_COMP_OUT_R 0R2-PT5-LILY-GP-U

3D3V_S5

Q2606 T2N7002BK-2-GP

PURE_HW_SHUTDOWN_N

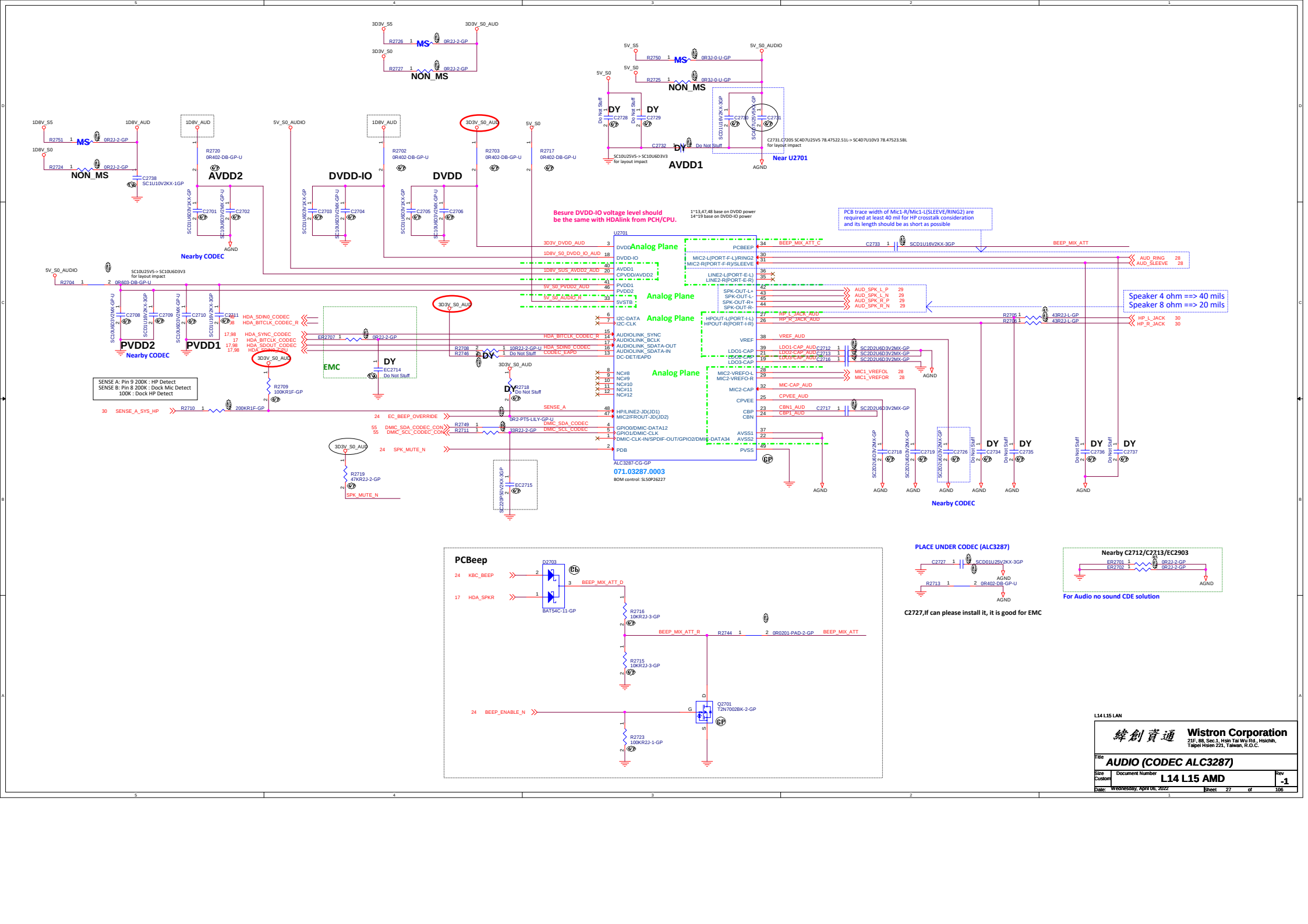
L14 L15 LAN

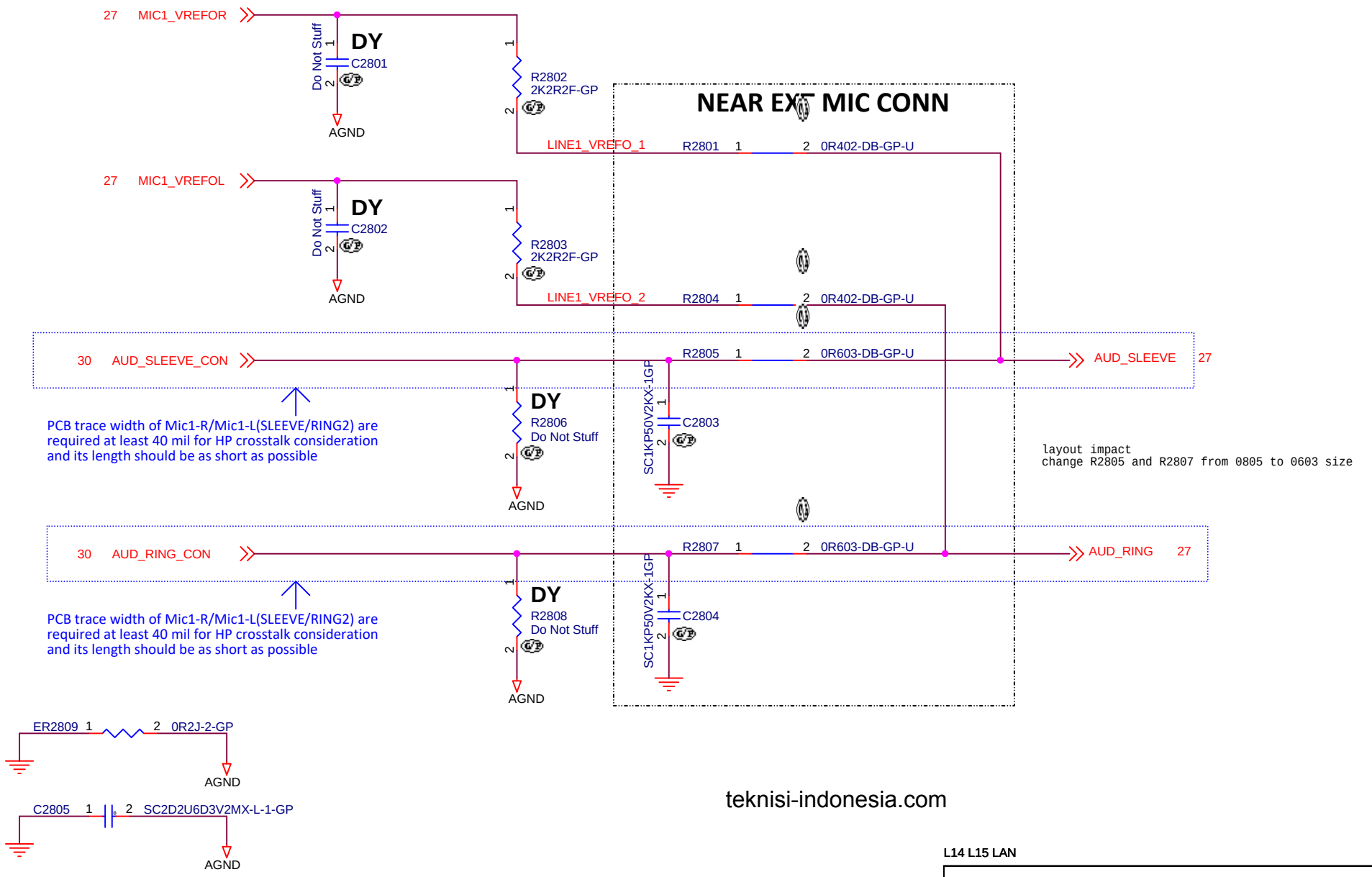
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (THERMAL/FAN)

Size: A2 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 26 of 106


3D3V_S5
3D3V_S0_AUD
R2726 MS 0R2J-2-GP
3D3V_S0
R2727 NON_MS 0R2J-2-GP
5V_S5
5V_S0_AUDIO
R2750 MS 0R3J-0-U-GP
5V_S0
R2725 NON_MS 0R3J-0-U-GP
DY C2728 C2729
SCD1U16V2KX-3GP C2730 C2731
SCA47U25V6KA-GP
C2731.C7205 SC4D7U25V5 78.47522.511-> SC4D7U10V3 78.47523.5BL for layout impact
C2732 DY Do Not Stuff
SC10U25V5-> SC10U6D3V3 for layout impact
Near U2701
AVDD1
AGND
1D8V_S5
1D8V_AUD
R2751 MS 0R2J-2-GP
1D8V_S0
R2724 NON_MS 0R2J-2-GP
C2738 SC1U10V2KX-1GP
R2720 0R402-DB-GP-U
AVDD2
DVDD-IO
R2702 0R402-DB-GP-U
DVDD
R2703 0R402-DB-GP-U
R2717 0R402-DB-GP-U
C2701 C2702
C2703 C2704
C2705 C2706
SCD1U6D3V1KX-GP
SC10U6D3V2MX-GP-U
Nearby CODEC
Besure DVDD-IO voltage level should be the same with HDAlink from PCH/CPU.
1~13,47,48 base on DVDD power
14~19 base on DVDD-IO power
PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration and its length should be as short as possible
U2701
3D3V_DVDD_AUD
1D8V_S0_DVDD_IO_AUD
1D8V_SUS_AVDD2_AUD
5V_S0_PVDD2_AUD
5V_S0_AUDIO_A
Analog Plane
PCBEEP
MIC2-L(PORT-F-L)/RING2
MIC2-R(PORT-F-R)/SLEEVE
LINE2-L(PORT-E-L)
LINE2-R(PORT-E-R)
SPK-OUT-L+
SPK-OUT-L-
SPK-OUT-R+
SPK-OUT-R-
HPOUT-L(PORT-I-L)
HPOUT-R(PORT-I-R)
VREF
LDO1-CAP
LDO2-CAP
LDO3-CAP
MIC2-VREFO-L
MIC2-VREFO-R
MIC2-CAP
CPVEE
CBP
CBN
AVSS1
AVSS2
PVSS
BEEP_MIX_ATT_C
C2733 SCD1U16V2KX-3GP
BEEP_MIX_ATT
AUD_RING 28
AUD_SLEEVE 28
AUD_SPK_L_P 29
AUD_SPK_L_N 29
AUD_SPK_R_P 29
AUD_SPK_R_N 29
Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 20 mils
HP_L_JACK_AUD
HP_R_JACK_AUD
R2705 R2706 43R2J-L-GP
HP_L_JACK 30
HP_R_JACK 30
VREF_AUD
LDO1-CAP_AUD C2712 SC2D2U6D3V2MX-GP
LDO2-CAP_AUD C2713 SC2D2U6D3V2MX-GP
LDO3-CAP_AUD C2716 SC2D2U6D3V2MX-GP
MIC1_VREFOL 28
MIC1_VREFOR 28
MIC-CAP_AUD
CPVEE_AUD
CBN1_AUD C2717 SC2D2U6D3V2MX-GP
CBP1_AUD
C2718 C2719 C2726 SC2D2U6D3V2MX-GP
DY C2734 C2735 C2736 C2737
Do Not Stuff
Nearby CODEC
I2C-DATA
I2C-CLK
AUDIOLINK_SYNC
AUDIOLINK_BCLK
AUDIOLINK_SDATA-OUT
AUDIOLINK_SDATA-IN
DC-DET/EAPD
NC#8
NC#9
NC#10
NC#11
NC#12
HP/LINE2-JD(JD1)
MIC2/FROUT-JD(JD2)
GPIO0/DMIC-DATA12
GPIO1/DMIC-CLK
DMIC-CLK-IN/SPDIF-OUT/GPIO2/DMIC-DATA34
PDB
ALC3287-CG-GP
071.03287.0003
BOM control: SL50P26227
HDA_SDIN0_CODEC
HDA_BITCLK_CODEC_R
HDA_SYNC_CODEC
HDA_BITCLK_CODEC
HDA_SDOUT_CODEC
HDA_SPWR_CPU
ER2707 0R2J-2-GP
R2708 R2746 10R2J-2-GP-U DY Do Not Stuff
HDA_SDIN0_CODEC
CODEC_EAPD
PVDD2
PVDD1
Nearby CODEC
EMC
EC2714 Do Not Stuff
SENSE A: Pin 9 200K : HP Detect
SENSE B: Pin 8 200K : Dock Mic Detect
100K : Dock HP Detect
R2709 100KR1F-GP
R2710 200KR1F-GP
SENSE_A_SYS_HP
SENSE_A
R2718 Do Not Stuff
EC_BEEP_OVERRIDE
0R2-PT5-LILY-GP-U
DMIC_SDA_CODEC_CON
DMIC_SCL_CODEC_CON
R2749 R2711 33R2J-2-GP
DMIC_SDA_CODEC
DMIC_SCL_CODEC
SPK_MUTE_N
R2719 47KR2J-2-GP
EC2715
SC220P50V2KX-3GP
SC10U25V5-> SC10U6D3V3 for layout impact
R2704 0R603-DB-GP-U
SCD1U10V2KX-3GP
SCD1U10V2KX-GP-U
SC10U6D3V2MX-GP-U
C2708 C2709 C2710 C2711
PCBeep
D2703
KBC_BEEP
HDA_SPKR
BAT54C-11-GP
BEEP_MIX_ATT_D
R2716 10KR2J-3-GP
BEEP_MIX_ATT_R
R2744 0R0201-PAD-2-GP
R2715 10KR2J-3-GP
BEEP_ENABLE_N
Q2701 T2N7002BK-2-GP
R2723 100KR2J-1-GP
PLACE UNDER CODEC (ALC3287)
C2727 SCD01U25V2KX-3GP
R2713 0R402-DB-GP-U
C2727,If can please install it, it is good for EMC
Nearby C2712/C2713/EC2903
ER2701 ER2702 0R2J-2-GP
For Audio no sound CDE solution
L14 L15 LAN
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title AUDIO (CODEC ALC3287)
Size Custom
Document Number L14 L15 AMD
Rev -1
Date: Wednesday, April 06, 2022
Sheet 27 of 106



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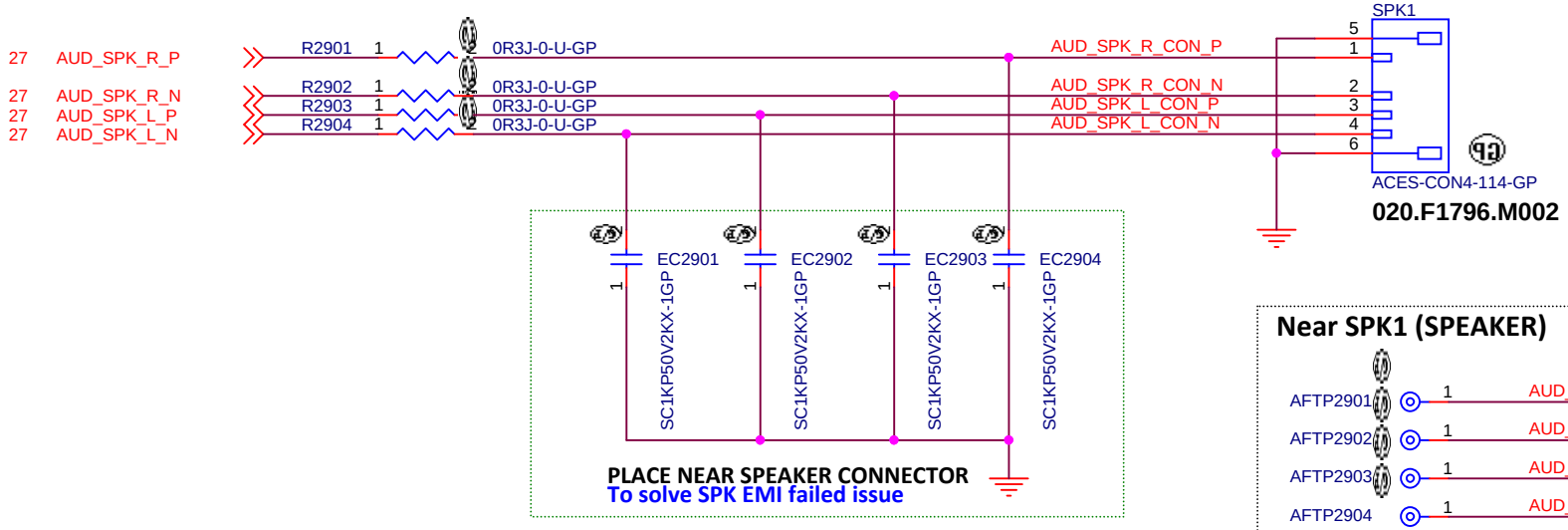
Title: AUDIO (MIC I/F)		
Size: A4	Document Number: L14 L15 AMD	Rev: -1
Date: Wednesday, April 06, 2022	Sheet 28 of 106	

SPEAKER CONN



L14 L15 LAN

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO (SPEAKER)*		
Size: A4	Document Number: L14 L15 AMD	Rev: -1
Date: Wednesday, April 06, 2022	Sheet 29 of 106	

NEAR AUDIO JACK CONN

27 HP_L_JACK → R3001 1 2 0R0201-PAD-2-GP

27 HP_R_JACK → R3002 1 2 0R0201-PAD-2-GP

C3002 SC100P50V2JN-L-GP 1 2

C3003 SC100P50V2JN-L-GP 1 2

Moat

Combo Jack

3D3V_S0_AUD → R3004 10KR2J-3-GP

AUD1

3	AUD_RING_CON
1	HP_L_JACK_CONN
5	3D3V_S0_HPJD
6	HP_JACK_SYS
2	HP_R_JACK_CONN
4	AUD_SLEEVE_CON
MS	

AUDIO-JK765-GP

022.10067.0071

FVT:022.10002.0W71-> 022.10067.0071

AUD_RING_CON HP_L_JACK_CONN → AUD_RING_CON 28

HP_JACK_SYS HP_R_JACK_CONN AUD_SLEEVE_CON → R3003 1 2 0R0201-PAD-2-GP

HP_JACK_IN 17

AUD_SLEEVE_CON 28

Close to AUD1 | Close to AUD1 | Close to AUD1

ED3001 PESD5V0U1BL-GP-U1 **83.0005V.CAF**

SC1KP50V2KX-1GP EC3006

Do Not Stuff EC3007 **DY**

ED3002 PESD5V0U1BL-GP-U1 **83.0005V.CAF**

ED3003 PESD5V0U1BL-GP-U1 **83.0005V.CAF**

ED3004 PESD5V0U1BL-GP-U1 **83.0005V.CAF**

ED3005 PESD5V0U1BL-GP-U1 **83.0005V.CAF**

Moat

83.0005V.CAF

83.05725.0A0 (075.05725.0073)

75.05125.07D-> 83.0005V.CAF
layout impact.

HGNDA/HGNDB trace width >70mil, changed to sharp will be better.

R3006 1 2 0R402-DB-GP-U

AGND

EC3005 1 2 SCD1U16V2KX-3GP

AGND

Moat

AUDIO JACK SENSE

CLOSE TO CODEC

6-10 mil trace recommend

AUDIO JACK SENSE

HP_JACK_SYS → R3005 22KR1J-GP → HP_JACK_SYS_R

R3010 100KR1J-GP → AGND

C3001 SC2D2U6D3V2MX-GP → AGND

Q3001 2N7002K-2-GP-U

G ← HP_JACK_SYS_R

S → AGND

D → SENSE_A_SYS_HP 27

84.2N702.J31

Near AUD1 (AUDIO)

AFTP3001	AUD_RING_CON
AFTP3002	HP_L_JACK_CONN
AFTP3003	3D3V_S0_HPJD
AFTP3004	HP_JACK_SYS
AFTP3005	HP_R_JACK_CONN
AFTP3006	AUD_SLEEVE_CON
AFTP3007	AGND

L14 L15 LAN

緯創資通 **Wistron Corporation**

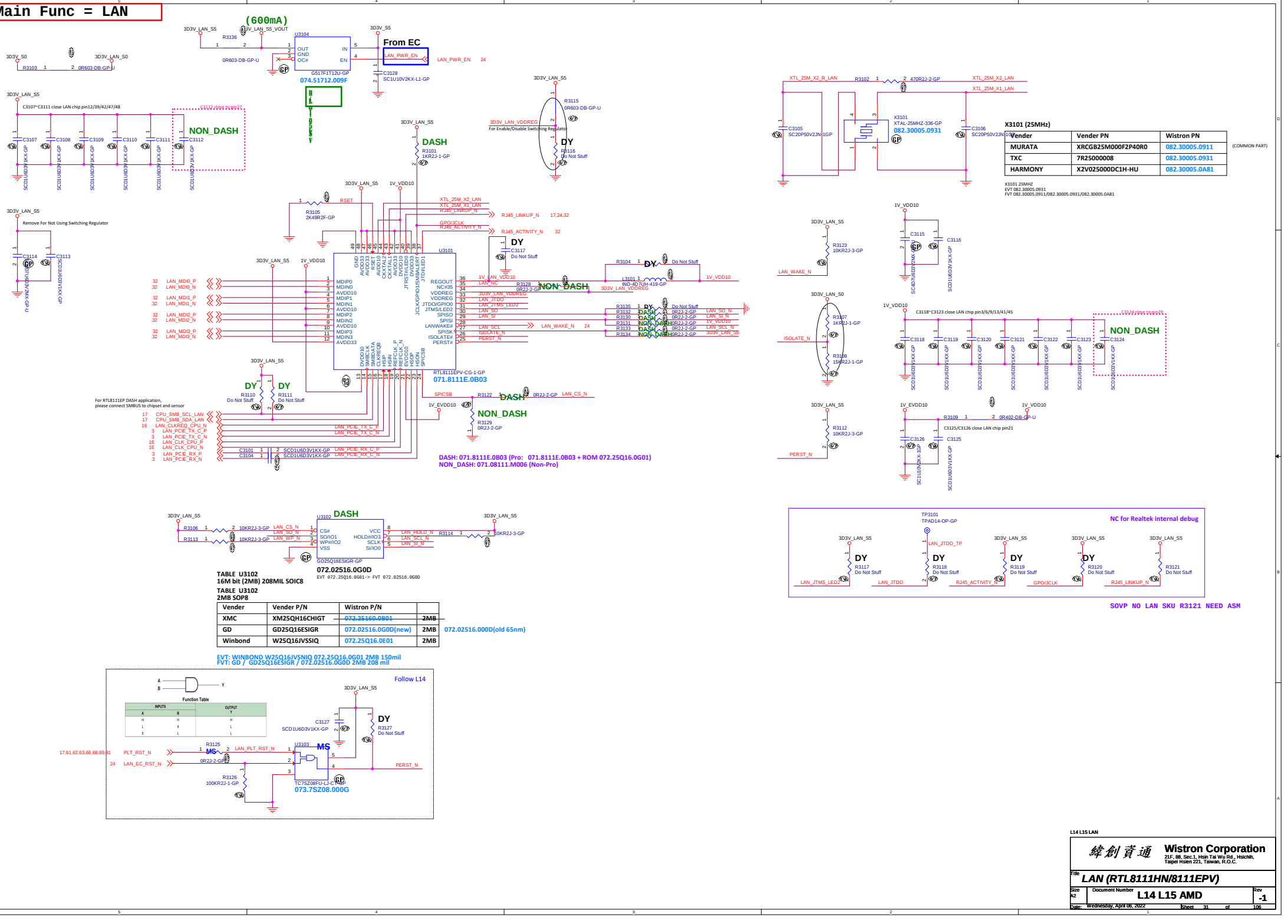
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO (AUDIO JACK)***

Size	Document Number	Rev
A3	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 30 of 106

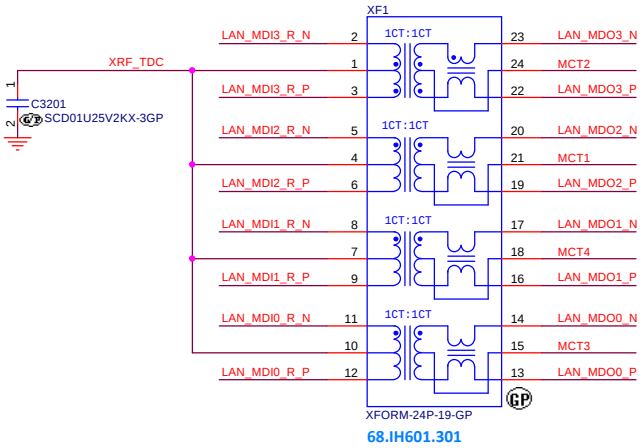
Main Func = LAN



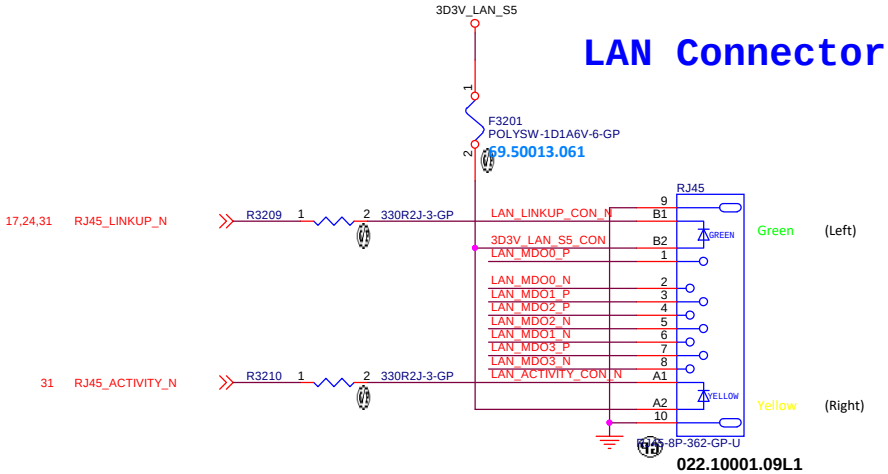
L14 L15 LAN

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LAN (RTL8111HN/8111EPV)
Size	A2
Document Number	L14 L15 AMD
Rev	-1
Date	Wednesday, April 06, 2022
Sheet	31 of 106

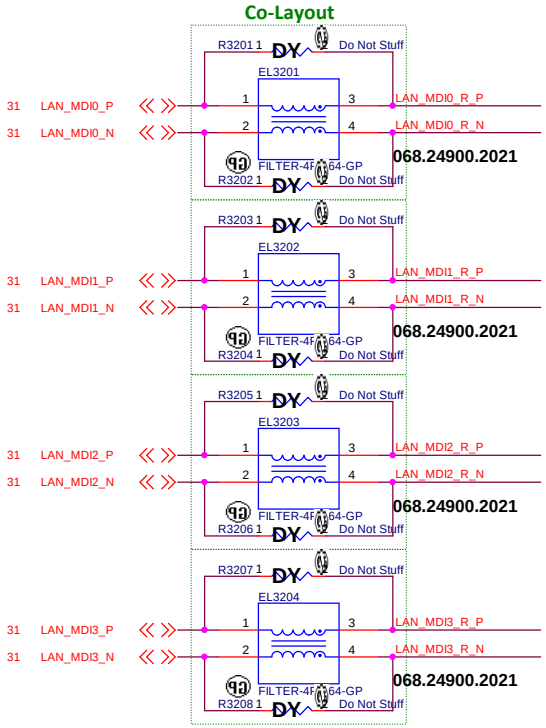
GIGA Lan Transformer

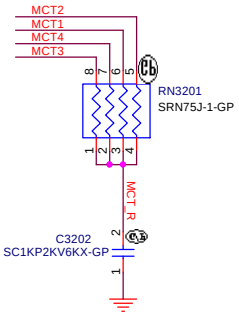


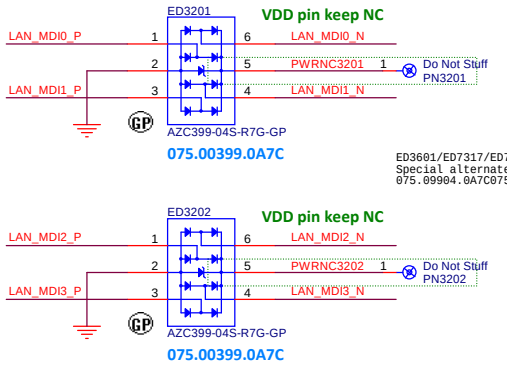
LAN Connector



Co-Layout







ED3601/ED7317/ED7417/ED9201 1st:075.09904.0A7C 2st:075.53456.000C 3st:075.54236.007C
Special alternate case for TVS DIODE shortage issue
075.09904.0A7C075.00199.007C075.08105.007C

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L14 L15 LAN

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 032_LAN (Transformer/LAN)

Size: A3 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 32 of 106

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L14 L15 LAN

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Title: ***CARD READER (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 33 of 106

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L14 L15 LAN

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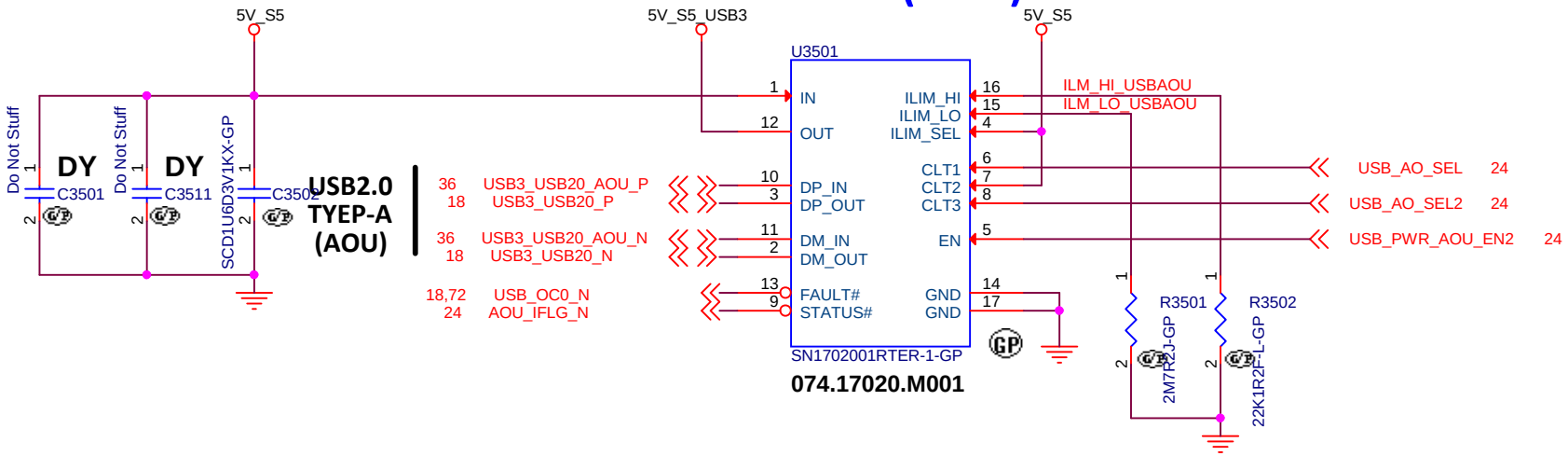
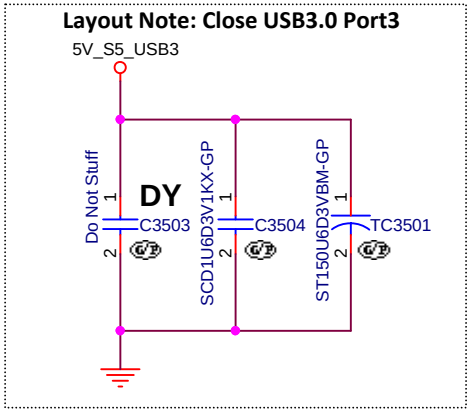
Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 34 of 106

USB3 TYPE-A (AOU) PWR





SN1702001RTER is not equivalent device of TPS2546RTER
Current Limit Target : 2.3A (2.1-2.45A)
TABLE of AOU port: U3501

Vendor	Vendor P/N	Wistron P/N	DS P/N
TI	SN1702001RTER (PG 1.1)	074.17020.M001	SL50Q67167AA
Pericom	PI5USB2546HZHEX	~~074.52546.0D73 (OBS)~~	~~SL50Q67168AA~~
Cellwise	CW3048BAAQ	074.03046.M001	SL81D97931AA
Diodes	PI5USB2546JZHEX		SL81C81273AA

L14 L15 LAN

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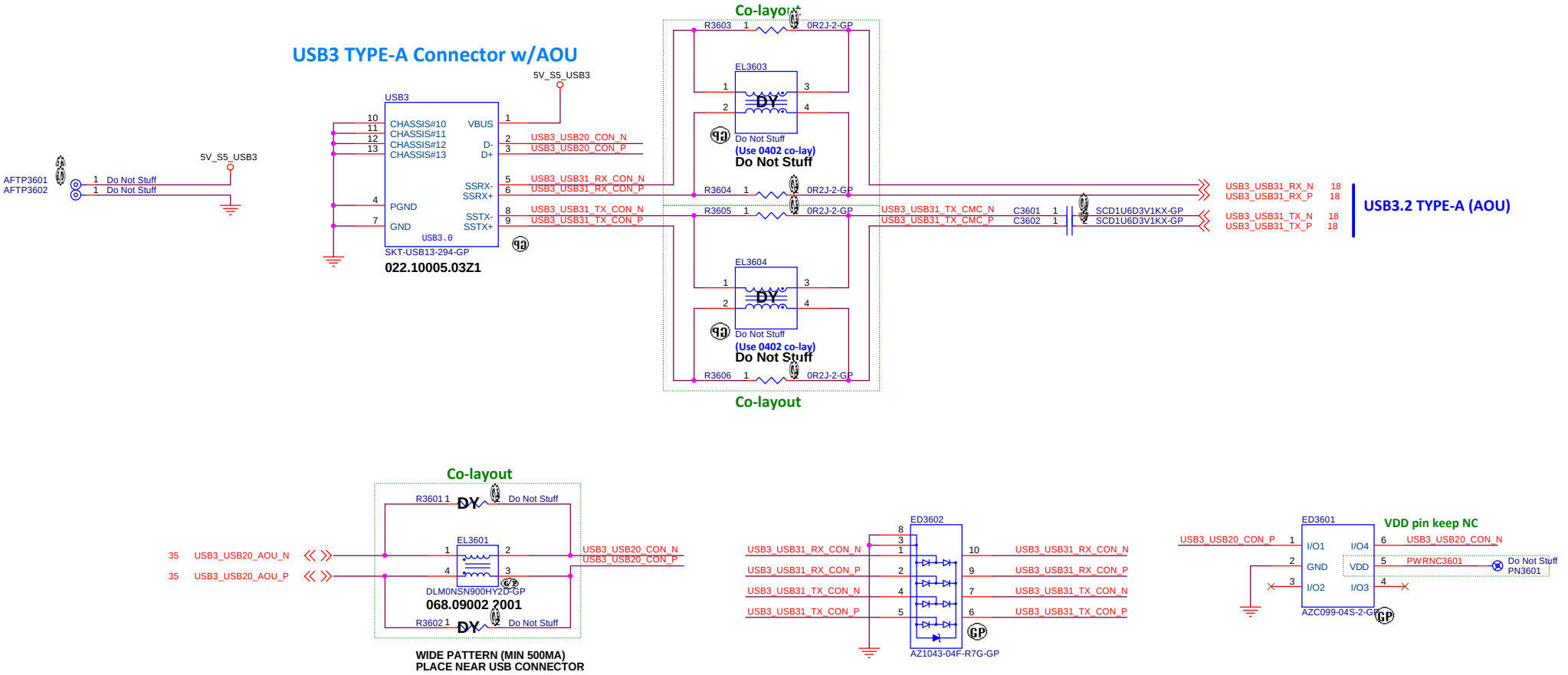
Title: **USB (CHARGER/SWITCH)**

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 35 of 106



L14 L15 LAN

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB (USB3.0 CONN)**

Size	Document Number	Rev
A3	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 36 of 106

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Title: ***USB (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 37 of 106

USB2 HUB

Power

3D3V_S0 — R3821 1 — DY — Do Not Stuff — 3D3V_HUB_VDD

3D3V_S5 — R3801 1 — DY — Do Not Stuff — 3D3V_HUB_VDD

C3801 SCD1U16V2KX-3GP — Close to pin 28

HUB

USB2.0 | 18 HUB_USB20_P | 18 HUB_USB20_N

Smart card

USB2.0 | 94 SMARTCAD_USB20_P | 94 SMARTCAD_USB20_N

CCD

USB2.0 | 55 CCD_USB20_CON_P | 55 CCD_USB20_CON_N

3D3V_S5 — R3824 330KR1J-GP — C3814 SCD1U16V2KX-3GP — Q3801 SSM3J327R-GP 84.03327.031 — 3D3V_S5 — 3D3V_HUB_V33

24 HUB_EC_PWRON_N — R3823 1KR1F-GP — HUB_EC_EN_R_N — R3822 20KR1J-GP — HUB_EC_EN_G_N

U3802 — 3D3V_HUB_VDD — HUB_I2C_SCL — HUB_I2C_SDA

Do Not Stuff

DY

EVT ASM

L3801 068.00017.0141 shortage-> 68.00206.211 (LAR-2)

3D3V_HUB_VDD — R3814 10KR2J-3-GP — OVCJ pin must be pulled high if not used. — C3812 SCD01U16V2KX-3GP

From USB3 HUB2

R3804 100KR2J-1-GP — 3D3V_HUB_BUSJ

HUB_OVCJ

R3805 100KR2J-1-GP — HUB_REXT

R3806 100KR2J-1-GP — 3D3V_HUB_VBUSM — 3D3V_HUB_XRSTJ

R3818 2K7R2F-GP +/-1%

25_THM

U3801

LED1 LED2 DPU DMU BUSJ DRV OVC# PWR# REXT TEST# VBUSM XRSTJ THERMAL_PAD

VDD5 VD33F DP1 DM1 DP2 DM2 DP3 DM3 DP4 DM4 XIN XOUT

FE1D1S-BQFN24B-GP

071.01124.0003

PWRNC3801 1 — Do Not Stuff PN3801

SMARTCAD_USB20_P — SMARTCAD_USB20_N — CCD_USB20_CON_P — CCD_USB20_CON_N

SCR

CCD

XTL_12M_X1_HUB — XTL_12M_X2_HUB

3D3V_HUB_VDD — C3810 SC22U16V3MX-GP-U

3D3V_HUB_VDD — 3D3V_HUB_V33 — L3801 MMZ1608Y471BTA00-GP 068.00017.0141

Bead 100MHz/470R/500mA

DCR=350~500mohm

L3801 068.00017.0141 SIT shortage
->BOM control to 68.00206.211 (same as LAR-2)
& add 2nd source

X3801 XTAL-12MHZ-136-GP 082.30000.0521

82.30006.491-> 082.30000.0291
TAITIEN 082.30000.0381
HARMONY 082.30000.0301
HOSONIC 082.30000.0291

Crystal spec. : Crystal 12MHZ/16~20pF, 30~50ppm,
ESR 50 ohm Max, Driver level 500uW Max
082.30000.0291-> 082.30000.0521

DY C3802 Do Not Stuff

DY C3803 Do Not Stuff

Co-Layout

R3825 0R2J-2-GP — L3802 DY — Do Not Stuff — Do Not Stuff — R3826 0R2J-2-GP

HUB_USB20_P — HUB_USB20_CMC_P

HUB_USB20_N — HUB_USB20_CMC_N

Do Not Stuff DY D3801

Do Not Stuff DY D3802

L14 L15 LAN

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**USB (USB REDRIVER/HUB)**
Size A3	Document Number **L14 L15 AMD** Rev **-1**
Date: Wednesday, April 06, 2022	Sheet 38 of 106

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L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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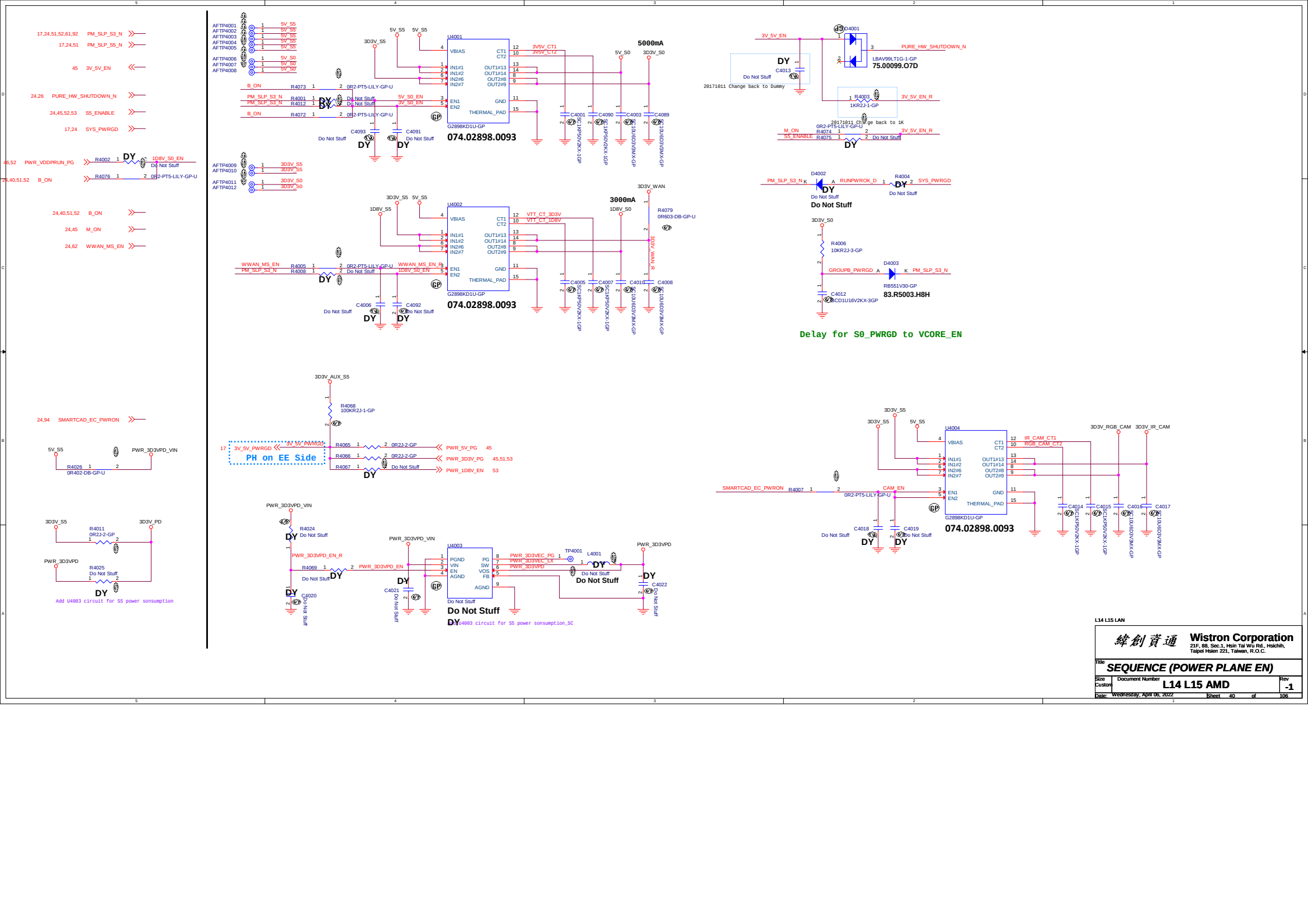
Title: ***SEQUENCE (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 39 of 106


17,24,51,52,61,92 PM_SLP_S3_N
17,24,51 PM_SLP_S5_N
45 3V_5V_EN
24,26 PURE_HW_SHUTDOWN_N
24,45,52,53 S5_ENABLE
17,24 SYS_PWRGD
46,52 PWR_VDDPRUN_PG
29,40,51,52 B_ON
24,40,51,52 B_ON
24,45 M_ON
24,62 WWAN_MS_EN
24,94 SMARTCAD_EC_PWRON
5V_S5
PWR_3D3VPD_VIN
R4026 0R402-DB-GP-U
3D3V_S5
3D3V_PD
R4011 0R2J-2-GP
PWR_3D3VPD
R4025 Do Not Stuff
DY
Add U4003 circuit for S5 power sonsumption
AFTP4001
AFTP4002
AFTP4003
AFTP4004
AFTP4005
AFTP4006
AFTP4007
AFTP4008
5V_S5
5V_S0
B_ON
R4073 0R2-PT5-LILY-GP-U
PM_SLP_S3_N
PM_SLP_S3_N
R4001 Do Not Stuff
R4012 Do Not Stuff
R4072 0R2-PT5-LILY-GP-U
5V_S0_EN
3V_S0_EN
U4001
VBIAS
IN1/#1
IN1/#2
IN2/#6
IN2/#7
EN1
EN2
CT1
CT2
OUT1/#13
OUT1/#14
OUT2/#8
OUT2/#9
GND
THERMAL_PAD
G2898KD1U-GP
3V5V_CT1
3V5V_CT2
5000mA
C4001 SC1KP50V2KX-1GP
C4090
C4003 1UU6D3V3MX-GP
C4089
C4093 Do Not Stuff
C4091 Do Not Stuff
074.02898.0093
AFTP4009
AFTP4010
AFTP4011
AFTP4012
3D3V_S5
3D3V_S0
U4002
1D8V_S5
1D8V_S0
WWAN_MS_EN
PM_SLP_S3_N
R4005 0R2-PT5-LILY-GP-U
R4008 Do Not Stuff
1D8V_S0_EN
VTT_CT_3D3V
VTT_CT_1D8V
3D3V_WAN
3000mA
R4079 0R603-DB-GP-U
C4005 SC1KP50V2KX-1GP
C4007 SC1KP50V2KX-1GP
C4010 1UU6D3V3MX-GP
C4008
C4006 Do Not Stuff
C4092 Do Not Stuff
074.02898.0093
3D3V_AUX_S5
R4068 100KR2J-1-GP
17
3V_5V_PWRGD
PH on EE Side
R4065 0R2J-2-GP
R4066 0R2J-2-GP
R4067 Do Not Stuff
PWR_5V_PG 45
PWR_3D3V_PG 45,51,53
PWR_1D8V_EN 53
PWR_3D3VPD_VIN
R4024 Do Not Stuff
PWR_3D3VPD_EN_R
R4069
PWR_3D3VPD_EN
U4003
PGND
VIN
EN
AGND
PG
SW
VOS
FB
PWR_3D3VEC_PG
PWR_3D3VEC_LX
PWR_3D3VPD
TP4001
L4001
Do Not Stuff
C4020 Do Not Stuff
C4021 Do Not Stuff
C4022 Do Not Stuff
U4003 circuit for S5 power sonsumption_SC
3V_5V_EN
D4001
LBAV99LT1G-1-GP
75.00099.O7D
PURE_HW_SHUTDOWN_N
C4013 Do Not Stuff
20171011 Change back to Dummy
R4003 1KR2J-1-GP
3V_5V_EN_R
20171011 Change back to 1K
M_ON
S5_ENABLE
R4074 0R2-PT5-LILY-GP-U
R4075 Do Not Stuff
D4002
PM_SLP_S3_N
RUNPWROK_D
R4004 Do Not Stuff
SYS_PWRGD
R4006 10KR2J-3-GP
GROUPB_PWRGD
D4003
PM_SLP_S3_N
RB551V30-GP
C4012 CD1U16V2KX-3GP
83.R5003.H8H
Delay for S0_PWRGD to VCORE_EN
SMARTCAD_EC_PWRON
R4007
CAM_EN
U4004
IR_CAM_CT1
RGB_CAM_CT2
3D3V_RGB_CAM
3D3V_IR_CAM
C4014
C4015
C4016
C4017
C4018 Do Not Stuff
C4019 Do Not Stuff
074.02898.0093
L14 L15 LAN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SEQUENCE (POWER PLANE EN)
Size Custom
Document Number
L14 L15 AMD
Rev -1
Date: Wednesday, April 06, 2022
Sheet 40 of 106

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L14 L15 LAN

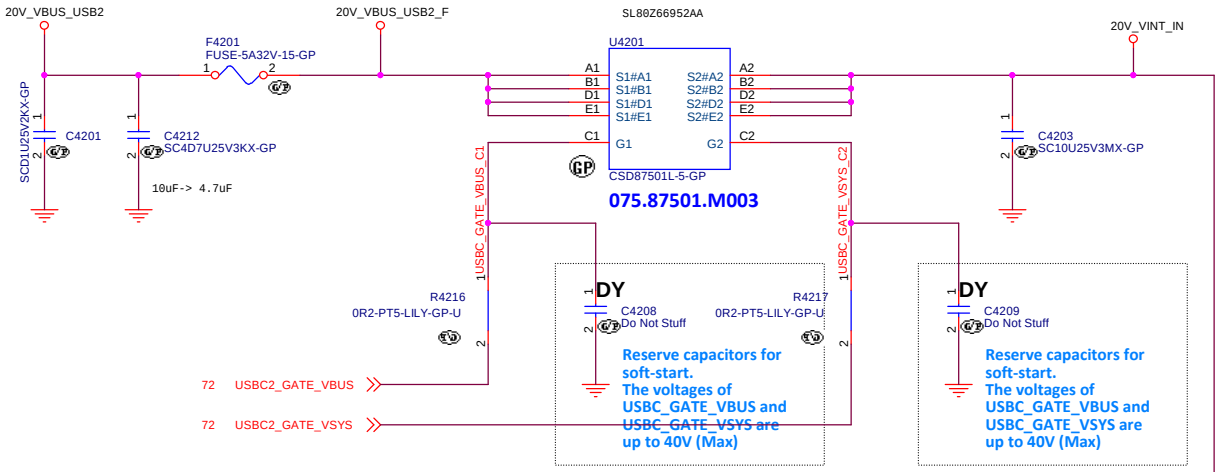
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

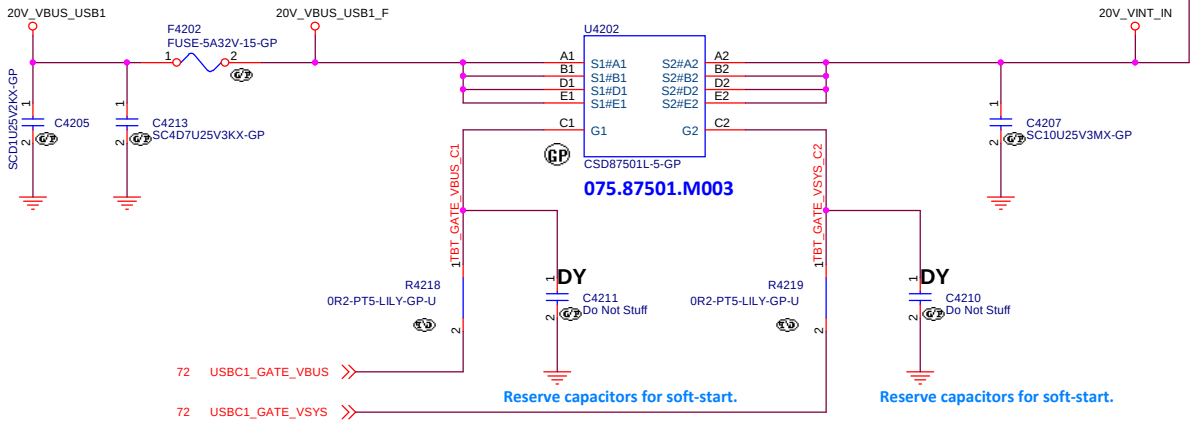
Title ***SEQUENCE (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 41 of 106

Main Func = ADT Input





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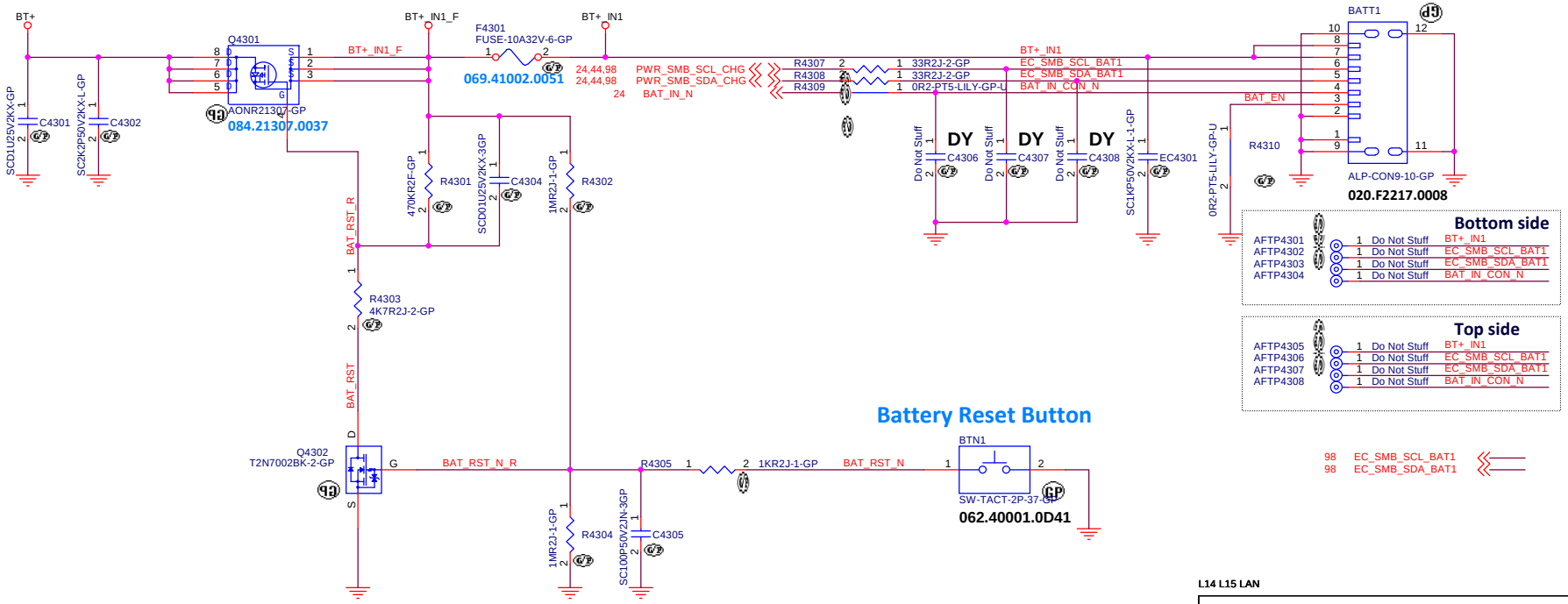
L14 L15 LAN

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *INT IO (TYPEC DC-DC)*		
Size: A3	Document Number: **L14 L15 AMD**	Rev: -1
Date: Wednesday, April 06, 2022	Sheet 42 of 106	



L14 L15 LAN

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***INT IO (ATX/ DC/ BATT CONN)***

Size	Document Number	Rev
Custom	**L14 L15 AMD**	-1

Date: Wednesday, April 06, 2022 Sheet 43 of 106

OFFPAGE - PIC - EE

PH on EE Side

24,43,98 PWR_SMB_SCL_CHG → PWR_SMB_SCL_CHG
24,43,98 PWR_SMB_SDA_CHG → PWR_SMB_SDA_CHG

PH on EE Side

8,24,46,72 PROCHOT_CPU_N → PROCHOT_CPU_N

24,44 ADP_I → R4401 → CHGR_PSYS_IMVP
24 AC_IN_N → DZQ-PTS-LILY-GP-U → AC_IN_N
24,44 ADP_I → R4402 (Do Not Stuff) → AD_IA

98 PWR_CHG_SCL
99 PWR_CHG_SDA

Device will be transition from normal Buck-Boost operation to PTM operation by:
- Set REGN3 [7] = 0, to disable the EN_EXITLIM.
- Set REGN3[6] = 1.
- Set REGN3[2:] = 1.
- Ground ILIM_HIZ pin.

Device will transition out of PTM mode with host control by:
- Set REGN3[2:] = 0.
- Pull ILIM_HIZ pin to high.
- Device exits PTM to buck-boost operation if tripping VINDPM or IINDPM.
- Device exits PTM to buck-boost operation under fault conditions (VCOC, TSHUT, BATOC).

PWR_SMB_SCL_CHG — PR4459 (Do Not Stuff) — PWR_CHG_SCL
PWR_SMB_SDA_CHG — PR4460 (Do Not Stuff) — PWR_CHG_SDA
AD_IA — PR4457 (Do Not Stuff) — PWR_CHG_IADP
PROCHOT_CPU_N — PR4458 (Do Not Stuff) — PWR_PROCHOT#_CPU
CHGR_PSYS_IMVP — PR4461 (Do Not Stuff) — PWR_CHGR_CHG_PSYS

BOM Control Table

LOGIC →

PU4401	PU4403 PU4405	PC4431 PC4432	PR4423	PC4401	PR4424	PC4473	PC4403	PR4412	PC4472	PC4412
BQ25710RSNR 074.25710.M004	Follow TABLE PU4403 PU4405	0.047uF (78.47322.2FL)	280K Ohm (64.28035.6DL)	1uF (78.10523.5FL)	16.9K Ohm (64.16925.6DL)	2200pF (78.22224.L0L)	33pF (78.33034.1FL)	10K Ohm (64.10025.6DL)	220pF (78.22124.2FL)	18pF (78.18034.1FL)
SC888LQDER 074.08885.M003	Only AONY36304 075.36304.0073	DY	226K Ohm (64.22635.6DL)	100pF (78.10134.L1L)	100K Ohm (64.10035.6DL)	DY	10pF (78.10034.L0L)	330K Ohm (64.33035.6DL)	DY	220pF (78.22124.2FL)

TABLE PU4403 PU4405 for BQ25710RSNR

Vender	Vender P/N	Wistron P/N
NIKO	PKC46DY	075.00046.0073
SINOPOWER	SM7321ESKPC-TRG	075.07321.0073
ROHM	HP8S36TB	075.08536.0073

4ZA.0P201.0001
4ZA.0P201.0002
4ZA.0P201.0003

TABLE PU4403 PU4405 for SC888LQDER

Vender	Vender P/N	Wistron P/N
AOS	AONY36304	075.36304.0073

For Adapter IN Confirm with EE

Acoustic noise reserve

PU4402 DSS8P2730F-3-GP

PU4403 FDMS3600-G2-RJK0215-COLAY-GP
ZZ.00215.037
1st = 075.36354.0073

PU4405 FDMS3600-G2-RJK0215-COLAY-GP
ZZ.00215.037
1st = 075.36354.0073

PL4401 IND-202UH-8S-GP-U1
2.2uH, DCR=18-20mohm, Idc=8A, Isat=14A 6.8*6.4*3mm
68.2R210.20B

PU4406 AON6291307-GP
084.21307.0037

PU4401 BQ25710RSNR-3-GP
074.25710.M004

PU4404 SC888LQDER-3-GP
084.88885.0037

PR4426 162k1-1-GP

PR4434 100KR2F-2-GP

PR4422 0R5R2-3-GP

PR4423 187KR2F-GP

PR4425 100KR22-1-GP

PR4430 137KR2F-1-GP

PC4433 SC100P50V2JN-1-GP

PR4424 16K9R2F-GP

PR4438 0R3R2F-GP

PR4421 0R3R2F-GP

PR4439 0R5R2-3-GP

PR4440 0R5R2-3-GP

PR4411 1R05F-L1-GP

PR4404 1R05F-L1-GP

PR4405 1R05F-L1-GP

PR4412 10KR2F-2-GP

PR4413 71KR2F-1-GP

PR4403 100KR2F-L1-GP

# of CELL	VCELL_PROT	PR4413
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

	VCLIM	PR4423
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	118K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

Reserve for Power test

Reserve for PTM If it hasn't more GPIO

$V_{PSYS} = R_{PSYS} \times K_{PSYS}(V_{ACP} \times I_{IN} + I_{BAT} \times I_{BAT})$

PC4401 SC100P50V2JN-1-GP
PC4402 SC100P50V2JN-1-GP
PC4403 SC100P50V2JN-1-GP
PC4404 SC100P50V2JN-1-GP
PC4405 SC100P50V2JN-1-GP
PC4406 SC100P50V2JN-1-GP
PC4407 SC100P50V2JN-1-GP
PC4408 SC100P50V2JN-1-GP
PC4409 SC100P50V2JN-1-GP
PC4410 SC100P50V2JN-1-GP
PC4411 SC100P50V2JN-1-GP
PC4412 SC1R5P50V2JN-1-GP
PC4413 SCD047U25V2KX-GP
PC4414 SCD047U25V2KX-GP
PC4415 SCD047U25V2KX-GP
PC4416 SCD010U5V2KX-1-GP
PC4417 SC100P50V2JN-1-GP
PC4418 SC100P50V2JN-1-GP
PC4419 SCD010U25V2KX-1-GP
PC4420 SC4R7U25V3KX-1-GP
PC4421 SC1R5P50V2JN-1-GP
PC4422 4P7U7V5M-AEP-TC
PC4423 SC4R7U25V3KX-1-GP
PC4424 SC4R7U25V3KX-1-GP
PC4425 SC100P50V2JN-1-GP
PC4426 SC100P50V2JN-1-GP
PC4427 SC100P50V2JN-1-GP
PC4428 SC100P50V2JN-1-GP
PC4429 SC100P50V2JN-1-GP
PC4430 SC100P50V2JN-1-GP
PC4431 SC100P50V2JN-1-GP
PC4432 SCD047U25V2KX-GP
PC4433 SC100P50V2JN-1-GP
PC4434 SCD047U25V2KX-GP
PC4435 SCD047U25V2KX-1-GP-U
PC4436 SC100P50V2JN-1-GP
PC4437 SC100P50V2JN-1-GP
PC4438 SC100P50V2JN-1-GP
PC4439 SC100P50V2JN-1-GP
PC4440 SC100P50V2JN-1-GP
PC4441 SC100P50V2JN-1-GP
PC4442 SC100P50V2JN-1-GP
PC4443 SC100P50V2JN-1-GP
PC4444 SC100P50V2JN-1-GP
PC4445 SC100P50V2JN-1-GP
PC4446 SC100P50V2JN-1-GP
PC4447 SC100P50V2JN-1-GP
PC4448 SC100P50V2JN-1-GP
PC4449 SC100P50V2JN-1-GP
PC4450 SC100P50V2JN-1-GP
PC4451 SCD047U25V2KX-GP
PC4452 SC100P50V2JN-1-GP
PC4453 SC100P50V2JN-1-GP
PC4454 SC100P50V2JN-1-GP
PC4455 SCD047U25V2KX-1-GP-U
PC4456 SC100P50V2JN-1-GP
PC4457 SC100P50V2JN-1-GP
PC4458 SC100P50V2JN-1-GP
PC4459 SC100P50V2JN-1-GP
PC4460 SC100P50V2JN-1-GP
PC4461 SC100P50V2JN-1-GP
PC4462 SC100P50V2JN-1-GP
PC4463 SC100P50V2JN-1-GP
PC4464 SC100P50V2JN-1-GP
PC4465 SC100P50V2JN-1-GP
PC4466 SC100P50V2JN-1-GP
PC4467 SC100P50V2JN-1-GP
PC4468 SC100P50V2JN-1-GP
PC4469 SC100P50V2JN-1-GP
PC4470 SC100P50V2JN-1-GP
PC4471 SC100P50V2JN-1-GP
PC4472 SC100P50V2JN-1-GP
PC4473 SC100P50V2JN-1-GP
PC4474 SCD010U10V2KX-1GP

PR4427 0R5R2-3-GP
PR4428 0R5R2-3-GP
PR4429 0R5R2-3-GP
PR4430 137KR2F-1-GP
PR4431 0R5R2-3-GP
PR4432 100KR22-1-GP
PR4433 0R5R2-3-GP
PR4434 100KR2F-2-GP
PR4435 0R5R2-3-GP
PR4436 0R5R2-3-GP
PR4437 13KR2F-GP
PR4438 0R3R2F-GP
PR4439 0R5R2-3-GP
PR4440 0R5R2-3-GP
PR4441 0R5R2-3-GP
PR4442 0R5R2-3-GP
PR4443 0R5R2-3-GP
PR4444 0R5R2-3-GP
PR4445 0R5R2-3-GP
PR4446 0R5R2-3-GP
PR4447 0R5R2-3-GP
PR4448 0R5R2-3-GP
PR4449 0R5R2-3-GP
PR4450 0R5R2-3-GP
PR4451 0R5R2-3-GP
PR4452 0R5R2-3-GP
PR4453 0R5R2-3-GP
PR4454 0R5R2-3-GP
PR4455 0R5R2-3-GP
PR4456 0R5R2-3-GP
PR4457 0R5R2-3-GP
PR4458 0R5R2-3-GP
PR4459 0R5R2-3-GP
PR4460 0R5R2-3-GP
PR4461 0R5R2-3-GP
PR4462 0R5R2-3-GP
PR4463 0R5R2-3-GP
PR4464 0R5R2-3-GP
PR4465 0R5R2-3-GP
PR4466 0R5R2-3-GP
PR4467 0R5R2-3-GP
PR4468 0R5R2-3-GP
PR4469 0R5R2-3-GP
PR4470 0R5R2-3-GP
PR4471 0R5R2-3-GP
PR4472 0R5R2-3-GP
PR4473 0R5R2-3-GP
PR4474 0R5R2-3-GP

PQ4404 DZQ-PTS-LILY-GP-U
84.2N702.J31

PT4401 (Do Not Stuff) DY
PT4402 DY

L14 L15 LAN

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (CHARGER_BQ25710R)
Size: Custom | Document Number: L14 L15 AMD | Rev: -1
Date: Wednesday, August 06, 2008 | Sheet 44 of 106

OFFPAGE-Signal

24,40,52,53 S5_ENABLE — R4501 Do Not Stuff — PWR_3D3V_EN
40,45 3V_5V_EN — R4502 Do Not Stuff
24,40 M_ON — R4505 0R2-PTS-LILY-GP-U
40,51,53 PWR_3D3V_PG

24 5V_EN — R4503 0R2-PTS-LILY-GP-U — PWR_5V_EN
40,45 3V_5V_EN — R4504 Do Not Stuff

PH on EE Side

40 PWR_5V_PG

OFFPAGE-GAP

19V_DCBATOUT — PWR_DCBATOUT_3D3V
PG4515 GAP-CLOSE-PWR-3-GP
PG4516 GAP-CLOSE-PWR-3-GP
PG4517 GAP-CLOSE-PWR-3-GP
PG4518 GAP-CLOSE-PWR-3-GP

3D3V_S5 — PWR_3D3V
PG4519 GAP-CLOSE-PWR-3-GP
PG4520 GAP-CLOSE-PWR-3-GP
PG4521 GAP-CLOSE-PWR-3-GP
PG4522 GAP-CLOSE-PWR-3-GP
PG4523 GAP-CLOSE-PWR-3-GP
PG4524 GAP-CLOSE-PWR-3-GP

3D3V_AUX_S5 — PWR_3D3V_LDO
PG4532
0R402-DB-GP-U

19V_DCBATOUT — PWR_DCBATOUT_5V
PG4552 GAP-CLOSE-PWR-3-GP
PG4553 GAP-CLOSE-PWR-3-GP
PG4555 GAP-CLOSE-PWR-3-GP
PG4557 GAP-CLOSE-PWR-3-GP
PG4559 GAP-CLOSE-PWR-3-GP
PG4561 GAP-CLOSE-PWR-3-GP

5V_S5 — PWR_5V
PG4551 GAP-CLOSE-PWR-3-GP
PG4554 GAP-CLOSE-PWR-3-GP
PG4556 GAP-CLOSE-PWR-3-GP
PG4558 GAP-CLOSE-PWR-3-GP
PG4560 GAP-CLOSE-PWR-3-GP
PG4563 GAP-CLOSE-PWR-3-GP
PG4564 GAP-CLOSE-PWR-3-GP
PG4566 GAP-CLOSE-PWR-3-GP

5V_AUX_S5 — PWR_5V_LDO
PG4565 GAP-CLOSE-PWR-3-GP

IDC : 6A
OCP : 8A

Hybrid/NVDC4串BT Need Change Solution

Vin Operating range : 4~24V
Vin_Max : 26V
Ilimt : 8A

PWR_3D3V_LDO — PR4516 Do Not Stuff — PWR_3D3V_VCC
PWR_3D3V_BOOT — PR4501 0R0603-PAD-1-GP-U — PWR_3D3V_BOOT_A — PC4506 SCD1U25V2KX-L-GP
PC4522 SC10U6D3V3MX-L-GP

PWR_DCBATOUT_3D3V
Close to PU4501
PC4503 SC10U6D3V3MX-L-GP
PC4502 SC10U6D3V3MX-L-GP
PC4513 SCD1U25V2KX-L-GP
PR4514 0R2J-1-GP

PU4501 TPS51393PRJER-GP
VIN, VIN, VIN, VIN
SW#6, SW#19, SW#20
NC#10, LDO, NC#16
EN, ENLDO
BOOT, PGOOD, FB, VOUT
GND, GND, GND, GND
074.51393.0A43

PWR_3D3V_EN, PWR_3D3V_EN2, PWR_3D3V_BOOT, PWR_3D3V_PG, PWR_3D3V_FB
PWR_3D3V_PH
PWR_3D3V_LDO_A
PR4515 0R2J-2-GP
PC4507 SC10U6D3V3MX-L-GP

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A
PL4501 IND-1D5UH-23-GP-U
68.1R510.10K
PWR_3D3V
PC4509 PC4510 PC4511 PC4512 SC22U6D3V3MX-L-GP
PC4514 Do Not Stuff

Place another side , make GND plan bigger

EN rating :5 .5V
ENLDO Rising Threshold :1.5V
ENLDO Falling Threshold : 0.8V
EN Rising Threshold :1.3V
EN Falling Threshold : 1.12V

PWR_DCBATOUT_3D3V
PR4512 100KR2J-GP
PR4513 100KR2J-1-GP
DY PR4505 Do Not Stuff
3D3V_AUX_S5

Trace used 10 mil
PWR_3D3V_VOUT
Close to PC4511
PG4530 GAP-CLOSE-PWR-3-GP
PC4526 SC470P50V2KX-L-GP
PWR_3D3V_FB2
PR4506 240KR2F-L-GP
PWR_3D3V_PH
DY PR4517 Do Not Stuff
PWR_3D3V_SNB
DY PC4527 Do Not Stuff

BOM Control Table

	TPS51393PRJER	JW5168BQFNF	SYV768BRAC
PU4501	074.51393.0A43	074.05168.0043	074.00768.0043 SL81G98086AA
PR4515	0R / 0402 (63.R0034.1DL)	DY	DY
PR4516	DY	0R / 0402 (63.R0034.1DL)	0R / 0402 (63.R0034.1DL)
PC4507	10uF / 0603 (78.10610.L0L)	DY	DY
PC4526	470pF / 0402 (78.47124.L0L)	1000pF / 0402 (78.10224.L1L)	1000pF / 0402 (78.10224.L1L)
PR4506	240KR / 0402 (64.24035.6DL)	1KR / 0402 (64.10015.L3L)	1KR / 0402 (64.10015.L3L)

LOGIC
(JP Project only)

IDC:8A

Vin Operating range : 4~24V
Vin_Max : 26V
Ilimt : 8A

Hybrid/NVDC4串BT Need Change Solution

5V_AUX_S5 — PR4552 Do Not Stuff
Place another side , make GND plan bigger

PWR_DCBATOUT_5V
Close to PU4551
PC4555 SC10U25V5KX4-L-GP
PC4554 SC10U25V5KX4-L-GP
PC4564 SCD1U25V2KX-L-GP

PU4551 TPS51395PDJER-GP
VIN, VIN, VIN, VIN
NC#10, NC#16
VCC
PGOOD, BOOT
SW#6, SW#19, SW#20
VOUT, FB, LDO
EN, ENLDO
GND, GND, GND, GND
074.51395.0A43

PWR_5V_PG, PWR_5V_BOOT, PWR_5V_PH
PR4554 0R0603-PAD-1-GP-U
PC4553 SCD1U25V2KX-L-GP
PWR_5V_BOOT_A

Cyntec. 6.8 x7.3 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A
PL4551 IND-1D5UH-23-GP-U
PWR_5V
PC4556 PC4557 PC4558 PC4559 PC4560 PC4561 SC22U6D3V3MX-L1-GP
DY

Trace used 10 mil
PWR_5V_VOUT
PG4562 GAP-CLOSE-PWR-3-GP
PC4563 SC1KP50V2KX-L-1-GP
PR4555 324KR2F-GP
PWR_5V_FB, PWR_5V_FB_A
PWR_5V_LDO

PWR_5V_VCC, PWR_5V_EN, PWR_5V_EN2
PC4562 SC10U6D3V3MX-L-GP
PR4556 1MR2J-1-GP
PR4511 300KR2J-GP
PR4510 100KR2J-1-GP
PC4551 SC10U6D3V3MX-L-GP

PWR_5V_PH
DY PR4557 Do Not Stuff
PWR_5V_SNB
DY PC4566 Do Not Stuff

EN rating :5 .5V
ENLDO Rising Threshold :1.5V
ENLDO Falling Threshold : 0.8V
EN Rising Threshold :1.3V
EN Falling Threshold : 1.12V

L14 L15 LAN

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51393/TPS51395R_5V/3D3V
Size: A2
Document Number: L14 L15 AMD
Rev: -1
Date: Wednesday, April 06, 2022
Sheet 45 of 106

OFFPAGE

SVID

- 8,24,44,72 PROCHOT_CPU_N
- 8 SVID_ALERT_CPU_N
- 8 SVID_CLK_CPU
- 8 SVID_DATA_CPU

VCORE

- 47 PWR_VCORE_PWM1
- 47 PWR_VCORE_PWM2
- 47 PWR_VCORE_PWM3
- 47 PWR_VCORE_CS1
- 47 PWR_VCORE_CS2
- 47 PWR_VCORE_CS3
- 47 PWR_VCORE_VINSEN_VIN

VDDNB

- 48 PWR_VDDNB_PWM
- 48 PWR_VDDNB_CS

- 47,48 PWR_VCORE_VTEMP

- 8 VSSCORE_SENSE
- 8 VCCCORE_SENSE
- 8 VDDNB_SENSE

Enable EE check

- 40,52 PWR_VDDPRUN_PG
- 24 CPUCORE_ON

PH on EE Side

- 8,68 PWR_SVID_PWRGD
- 24 PWR_VCORE_VR_READY
- 24,26 PWR_VCORE_NB_READY

EE check

- 24,98 EC_SMB_SCL_BAT
- 24,98 EC_SMB_SDA_BAT

EE need confirm VCCIO

1DBV_S0 — PG4601 Do Not Stuff — PWR_VCORE_1D8V

PROCHOT_CPU_N — PR4642 0R402-DB-GP-U — PWR_VCORE_OCP_L

EC_SMB_SCL_BAT — PR4661 0R2J-2-GP — PWR_VCORE_SVC

EC_SMB_SDA_BAT — PR4662 0R2J-2-GP — PWR_VCORE_SVD

RSVD for tile beep option

PU4601 (MP2945GU-0013-C669-Z-GP, 074.02945.M009)

- PWR_VDDNB_CS
- PWR_VCORE_CS3
- PWR_VCORE_CS2
- PWR_VCORE_CS1
- PWR_VCORE_PWM1
- PWR_VCORE_PWM2
- PWR_VCORE_PWM3
- PWR_VDDNB_PWM
- PWR_VCORE_1D8V
- PWR_VCORE_DATA
- PWR_VCORE_CLK
- PWR_SVID_PWRGD
- PWR_VCORE_VCCIO
- PWR_VCORE_SVT
- PWR_VCORE_SVC
- PWR_VCORE_SVD
- PWR_VCORE_ALT_P_N
- PWR_VCORE_OCP_L
- 1V_CPU_CORE — PR4626 100R2F-L1-GP-U
- VCCCORE_SENSE — PR4627 0R402-DB-GP-U
- VSSCORE_SENSE — PR4628 0R402-DB-GP-U
- PR4629 100R2F-L1-GP-U
- PR4633 100R2F-L1-GP-U
- VSSCORE_SENSE — PR4631 0R402-DB-GP-U
- VDDSOC_SENSE — PR4632 0R402-DB-GP-U
- 1V_VDDCR_SOC — PR4630 100R2F-L1-GP-U
- PWR_VCORE_VTEMP — PR4634 0R402-DB-GP-U
- PWR_VCORE_CS1 — PR4623 1K5R2F-2-GP
- PWR_VCORE_CS2 — PR4624 1K5R2F-2-GP
- PWR_VCORE_CS3 — PR4625 1K5R2F-2-GP
- PWR_VDDNB_CS — PR4622 1K5R2F-2-GP
- PR4638 453R2F-1-GP
- PR4644 61K9R2F-GP
- PR4608 150KR2F-L-GP
- PR4609 10KR2F-2-GP
- PR4605 10K9R2F-L-GP
- PR4636 10K9R2F-L-GP
- PR4607 4D7R3F-L-GP
- PR4606 10KR2F-2-GP
- PR4643 10KR2F-2-GP
- PR4610 2D2R2F-GP
- PR4612 Do Not Stuff
- PR4613 Do Not Stuff
- PR4619 Do Not Stuff
- PR4601 Do Not Stuff
- PR4620 Do Not Stuff
- PR4621 0R0402-PAD-1-GP
- PR4650 0R0402-PAD-1-GP
- PR4651 0R0402-PAD-1-GP
- PR4656 Do Not Stuff
- PR4611 1K33R2F-GP
- PC4601 Do Not Stuff
- PC4610 Do Not Stuff
- PC4611 Do Not Stuff
- PC4612 SCD01U25V2KX-L1-GP
- PC4613 SCD01U25V2KX-L1-GP
- PC4614 Do Not Stuff
- PC4602 Do Not Stuff
- PC4603 SCD01U25V2KX-L1-GP
- PC4604 SC1U10V2KX-L1-GP
- PC4605 SCD01U25V2KX-L1-GP
- PC4606 SC1U10V2KX-L1-GP
- PC4607 SCD01U25V2KX-L-GP
- PC4609 SC1U10V2KX-L1-GP
- 3D3V_S5
- 41_THM

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L14 L15 LAN

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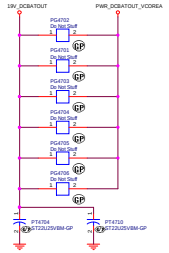
Title	MP2945_VCORE(1/3)
Size: Custom	Document Number: L14 L15 AMD
Rev	-1
Date: Wednesday, April 06, 2022	Sheet 45 of 106

OFFPAGE



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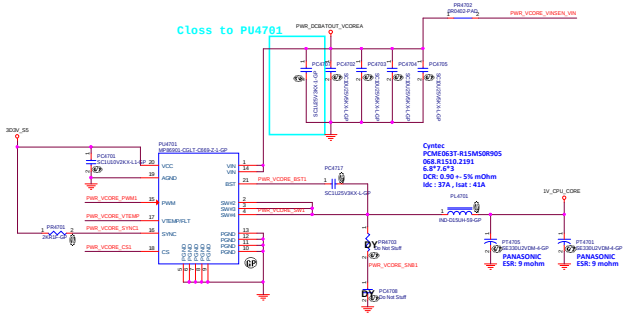

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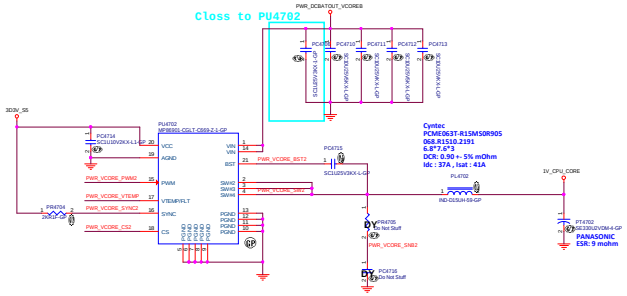

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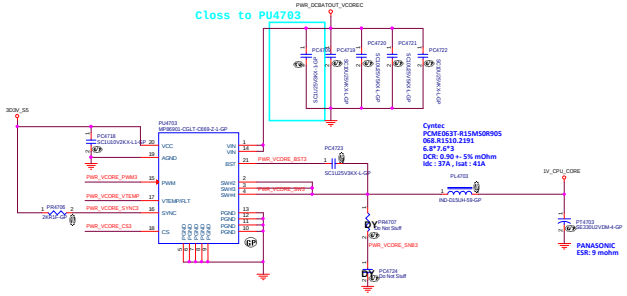


FP6 15W
CPU_CORE
TDC : 33A
Iccmax : 90A
OCP < 112.5A

Table 8. FP6 Processor Voltage Supply Currents for AMD Family 19h Models 50h-5Fh Processors

Supply [1]	Nominal Voltage at Pkg Ball (V) [2]	Condition	SYSTEM_CONFIGURATION					
			1 10 W	2 15 W	3 25 W	4 35 W	5 45 W	6 54 W
VDDCR_VDD	Variable (0.6-1.55) [5]	TDC [3]	20	33	44	51		58
		EDC	70	90	95	105		110
		Max Loadstep [4]	60	75	80	90		95
VDDCR_SOC	Variable (0.6-1.55) [5]	TDC [3]	10	13				15
		EDC	13	17				20
		Max Loadstep [4]	10	13				15
	1.10	TDC			6.00			

L14 L15 LAN

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	MP86901_VCORE(2/3)
Size	
Document Number	L14 L15 AMD
Rev	-1
Date: Wednesday, April 06, 2022	Sheet 47 of 55

OFFPAGE

19V_DCBATOUT PWR_DCBATOUT_VDDSOC

PG4802 PG4803 PG4804 PG4801 PG4805 PG4806

GAP-CLOSE-PWR-GP

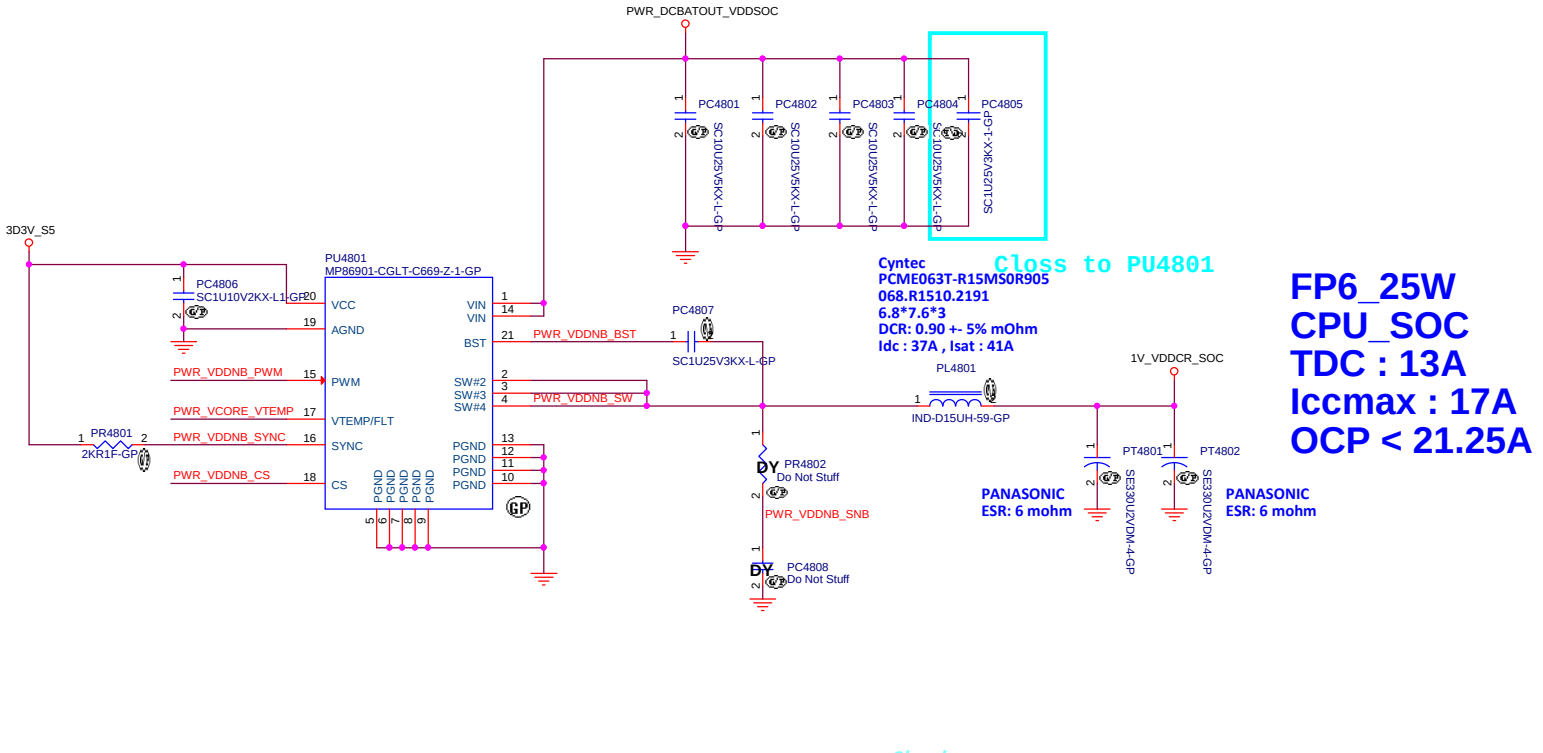
46 PWR_VDDNB_PWM

46,47 PWR_VCORE_VTEMP

46 PWR_VDDNB_CS

Main Func = CPU_CORE

Main Func = CPU_CORE



L14 L15 LAN

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *MP86901_VDDCR_SOC(3/3)*		
Size: Custom	Document Number: L14 L15 AMD	Rev: -1
Date: Wednesday, April 06, 2022	Sheet 48 of 106	

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L14 L15 LAN

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Title: ***Power (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	-1

Date: Wednesday, April 06, 2022 Sheet 49 of 106

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L14 L15 LAN

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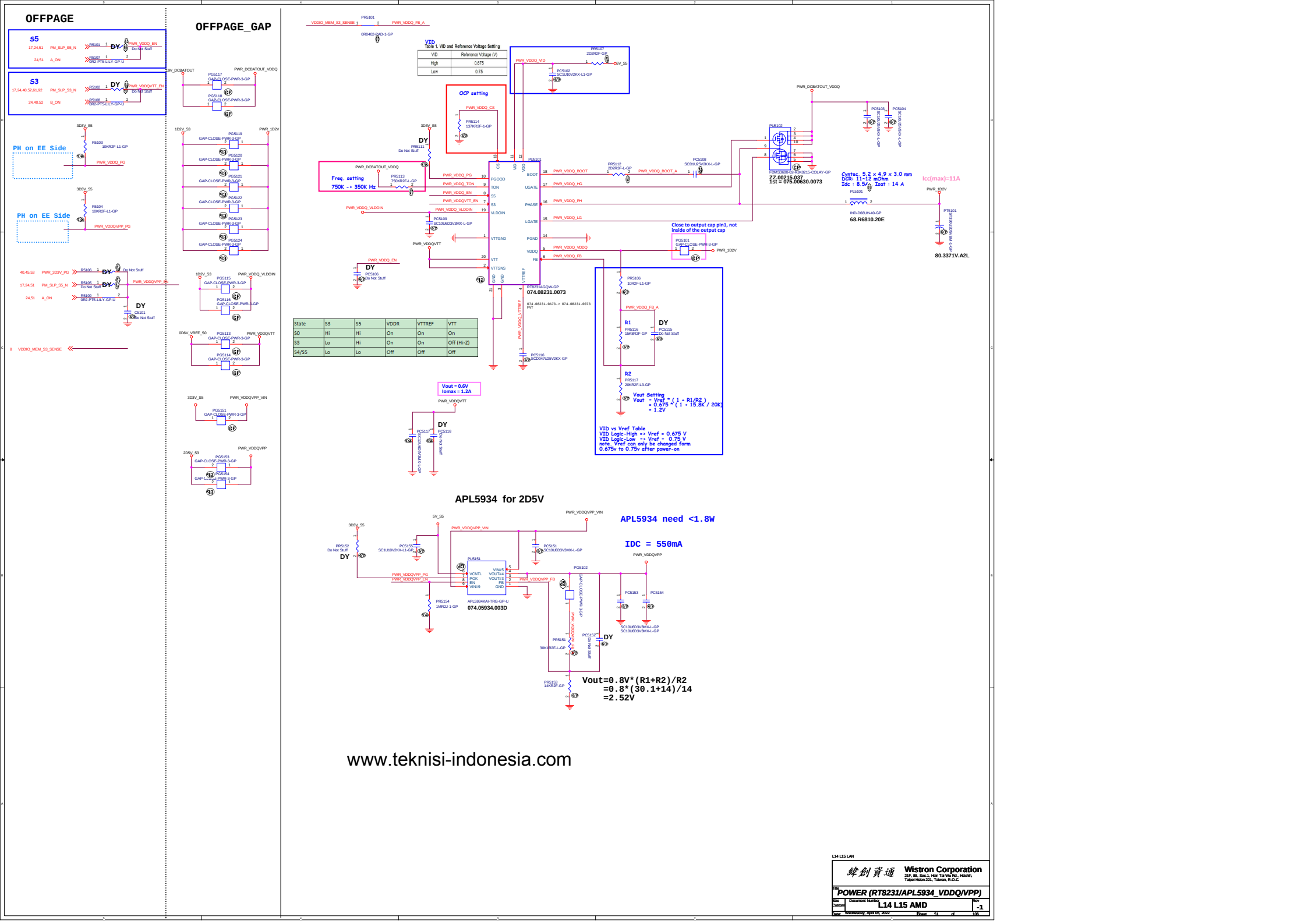
Title: ***Power (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	-1

Date: Wednesday, April 06, 2022 Sheet 50 of 106


OFFPAGE
S5
S3
PH on EE Side
PH on EE Side
OFFPAGE_GAP
VID
Table 1. VID and Reference Voltage Setting
VID | Reference Voltage (V)
High | 0.675
Low | 0.75
OCP setting
Freq. setting
750K -> 350K Hz
Close to output cap pin1, not inside of the output cap
State | S3 | S5 | VDDR | VTTREF | VTT
S0 | Hi | Hi | On | On | On
S3 | Lo | Hi | On | On | Off (Hi-Z)
S4/S5 | Lo | Lo | Off | Off | Off
Vout = 0.6V
Iomax = 1.2A
VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form 0.675v to 0.75v after power-on
APL5934 for 2D5V
APL5934 need <1.8W
IDC = 550mA
Vout=0.8V*(R1+R2)/R2
=0.8*(30.1+14)/14
=2.52V
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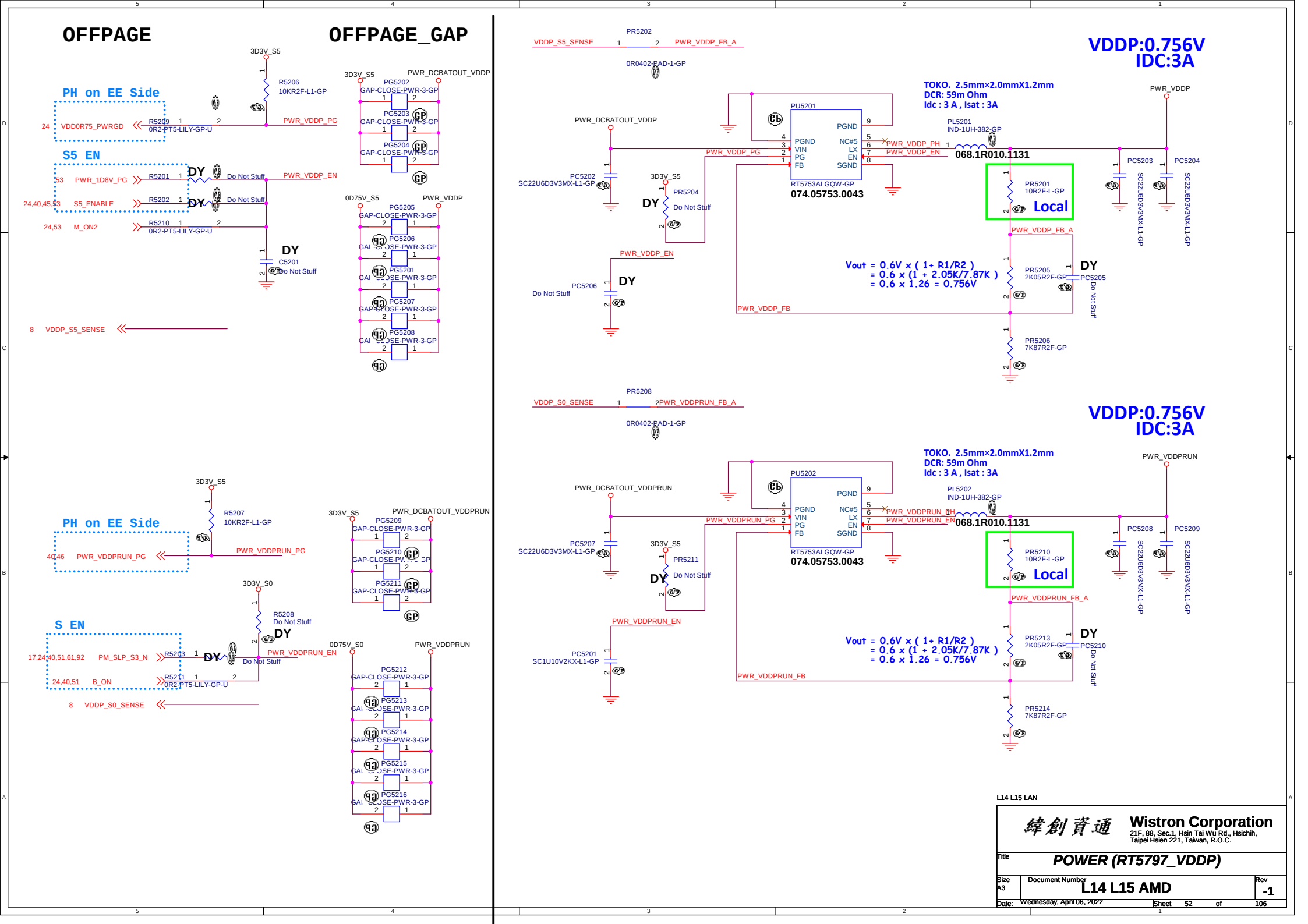
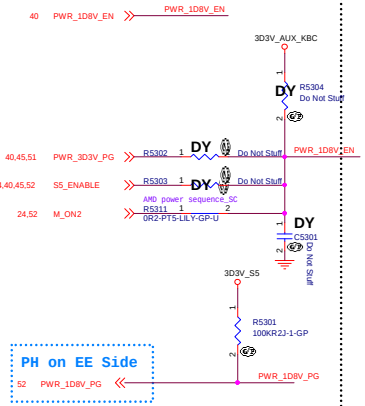
POWER (RT8231/APL5934_VDDQ/VPP)
L14 L15 AMD


OFFPAGE
OFFPAGE_GAP
PH on EE Side
S5 EN
S EN
VDDP:0.756V
IDC:3A
TOKO. 2.5mm×2.0mmX1.2mm
DCR: 59m Ohm
Idc : 3 A , Isat : 3A
068.1R010.1131
074.05753.0043
RT5753ALGQW-GP
Local
Vout = 0.6V x (1+ R1/R2)
= 0.6 x (1 + 2.05K/7.87K)
= 0.6 x 1.26 = 0.756V
Do Not Stuff
L14 L15 LAN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
POWER (RT5797_VDDP)
L14 L15 AMD
Wednesday, April 06, 2022
52
106

OFFPAGE-Signal



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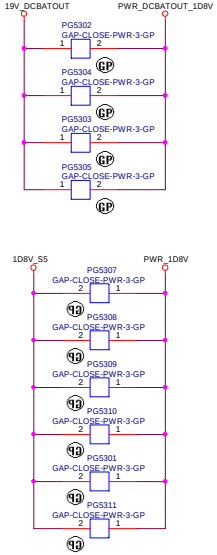

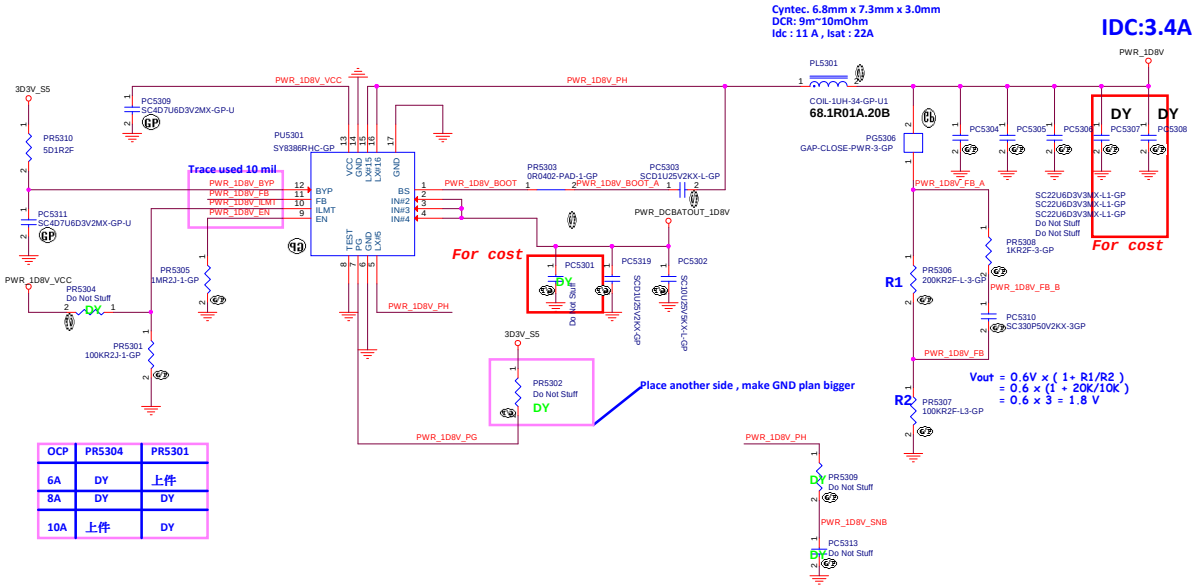

OCP	PR5304	PR5301
6A	DY	上件
8A	DY	DY
10A	上件	DY

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Title: ***POWER(SY8386R_1D8V)***

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Date: Wednesday, April 06, 2022 | Sheet 53 of 106

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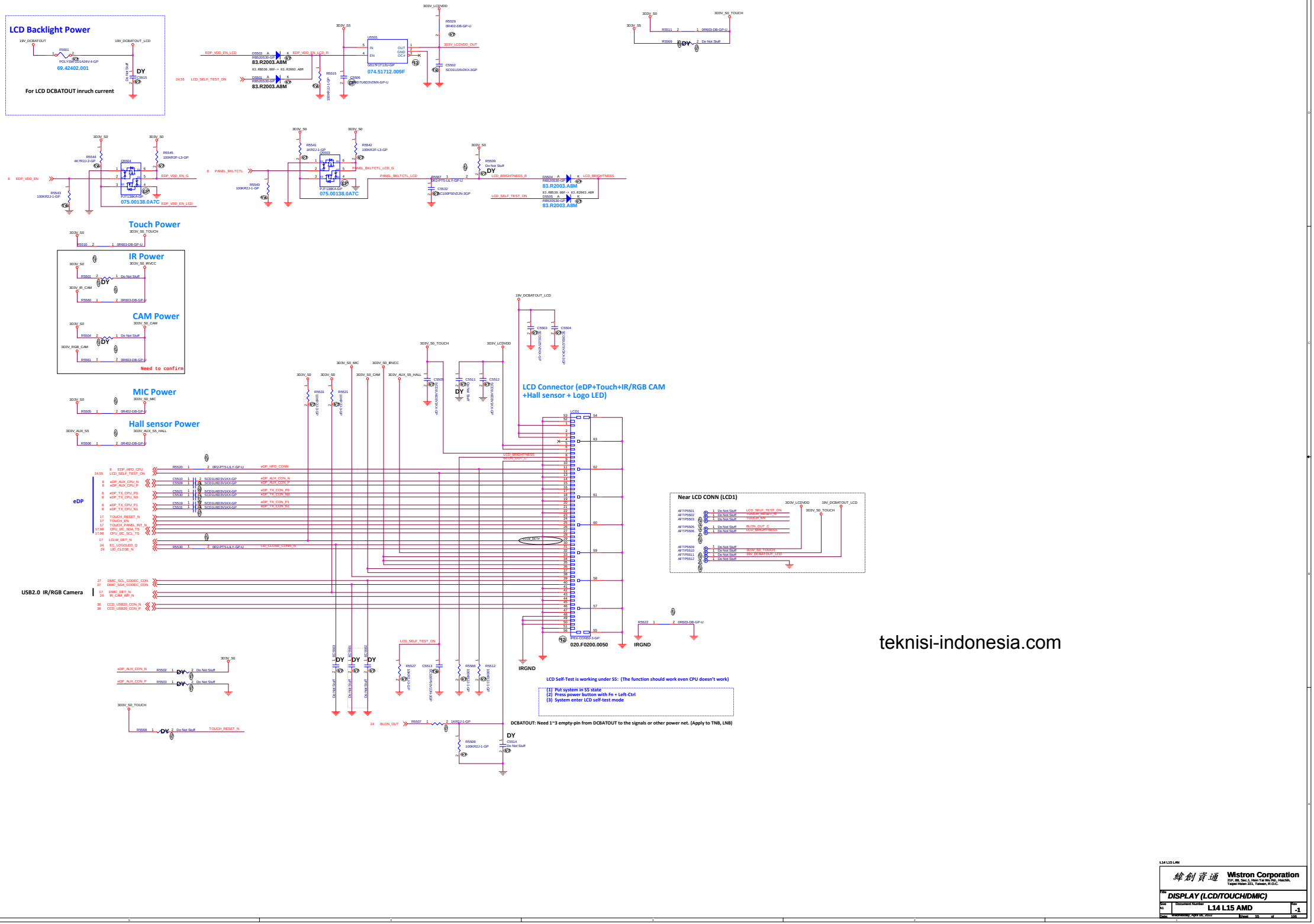
Title: ***POWER(RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 54 of 106



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Title: DISPLAY (LCD/TOUCH/DMIC)

Size: N1 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 08, 2009 | Sheet 55 of 105

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L14 L15 LAN

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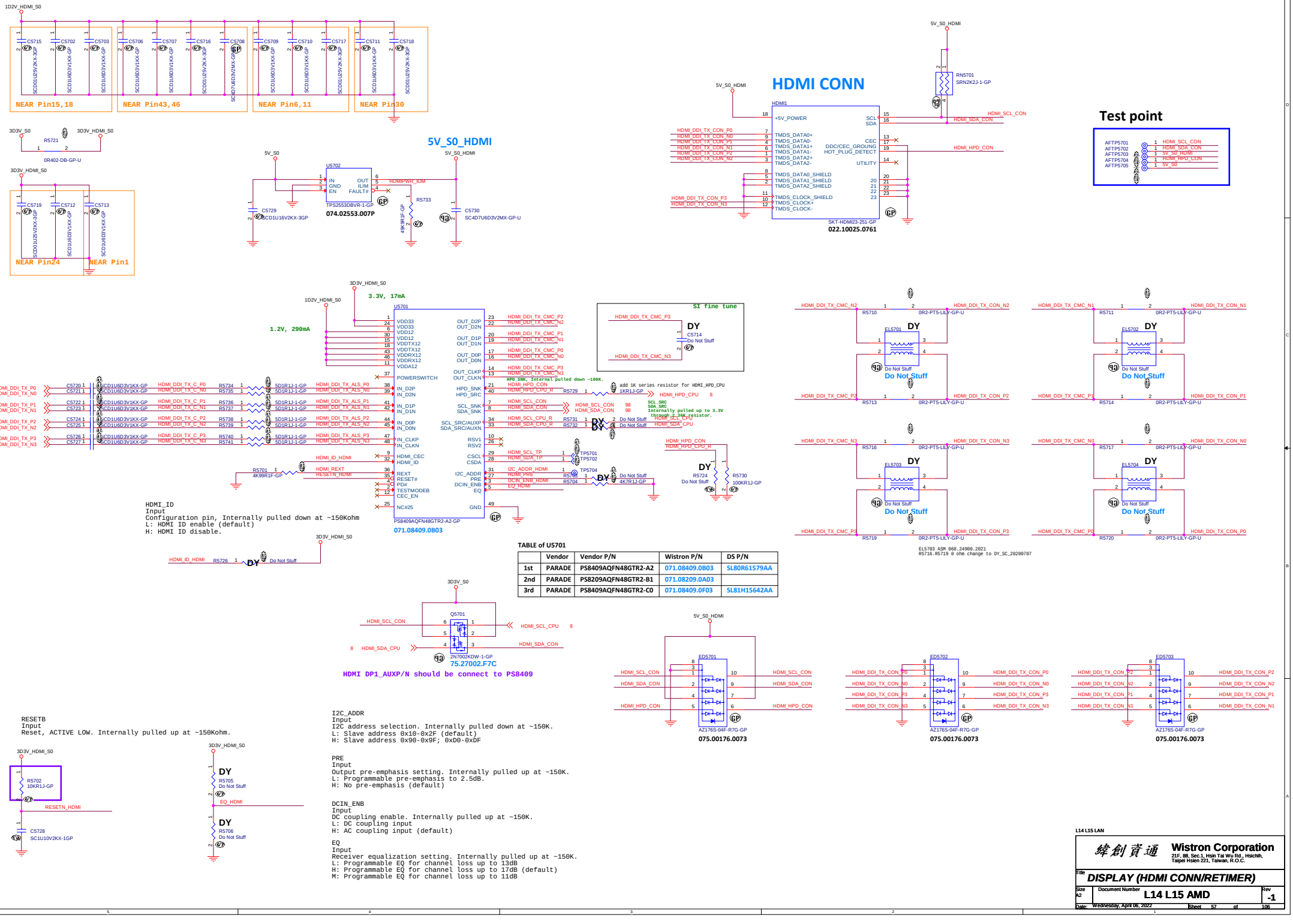
Title: ***DISPLAY (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 56 of 106


1D2V_HDMI_S0
NEAR Pin15,18
NEAR Pin43,46
NEAR Pin6,11
NEAR Pin30
3D3V_S0
3D3V_HDMI_S0
R5721
0R402-DB-GP-U
NEAR Pin24
NEAR Pin1
5V_S0_HDMI
5V_S0
U5702
TPS2553DBVR-1-GP
074.02553.007P
HDMI CONN
HDMI1
SKT-HDMI23-251-GP
022.10025.0761
RN5701
SRN2K2J-1-GP
Test point
AFTP5701
AFTP5702
AFTP5703
AFTP5704
AFTP5705
U5701
PS8409AQFN48GTR2-A2-GP
071.08409.0B03
3.3V, 17mA
1.2V, 290mA
SI fine tune
HPD_SNK, Internal pulled down ~100K.
add 1K series resistor for HDMI_HPD_CPU
SCL_SRC
SDA_SRC
Internally pulled up to 3.3V through 2.2K resistor.
HDMI_ID
Input
Configuration pin, Internally pulled down at ~150Kohm
L: HDMI ID enable (default)
H: HDMI ID disable.
TABLE of U5701
Vendor
Vendor P/N
Wistron P/N
DS P/N
1st PARADE PS8409AQFN48GTR2-A2 071.08409.0B03 SL80R61579AA
2nd PARADE PS8209AQFN48GTR2-B1 071.08209.0A03
3rd PARADE PS8409AQFN48GTR2-C0 071.08409.0F03 SL81H15642AA
Q5701
2N7002KDW-1-GP
75.27002.F7C
HDMI DP1_AUXP/N should be connect to PS8409
EL5701 ASM 068.24900.2021
R5716.R5719 0 ohm change to DY_SC_20200707
ED5701
ED5702
ED5703
AZ176S-04F-R7G-GP
075.00176.0073
RESETB
Input
Reset, ACTIVE LOW. Internally pulled up at ~150Kohm.
I2C_ADDR
Input
I2C address selection. Internally pulled down at ~150K.
L: Slave address 0x10-0x2F (default)
H: Slave address 0x90-0x9F; 0xD0-0xDF
PRE
Input
Output pre-emphasis setting. Internally pulled up at ~150K.
L: Programmable pre-emphasis to 2.5dB.
H: No pre-emphasis (default)
DCIN_ENB
Input
DC coupling enable. Internally pulled up at ~150K.
L: DC coupling input
H: AC coupling input (default)
EQ
Input
Receiver equalization setting. Internally pulled up at ~150K.
L: Programmable EQ for channel loss up to 13dB
H: Programmable EQ for channel loss up to 17dB (default)
M: Programmable EQ for channel loss up to 11dB
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Title
DISPLAY (HDMI CONN/RETIMER)
Size A2
Document Number
L14 L15 AMD
Rev -1
Date: Wednesday, April 06, 2022
Sheet 57 of 106

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Title: ***DISPLAY (RSVD)***

Size	Document Number	Rev
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Date: Wednesday, April 06, 2022 Sheet 58 of 106

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Title: ***DISPLAY (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 59 of 106

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Title: *INT IO (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 60 of 106

Main Func = WLAN

V2 Modern Standby CIRCUIT

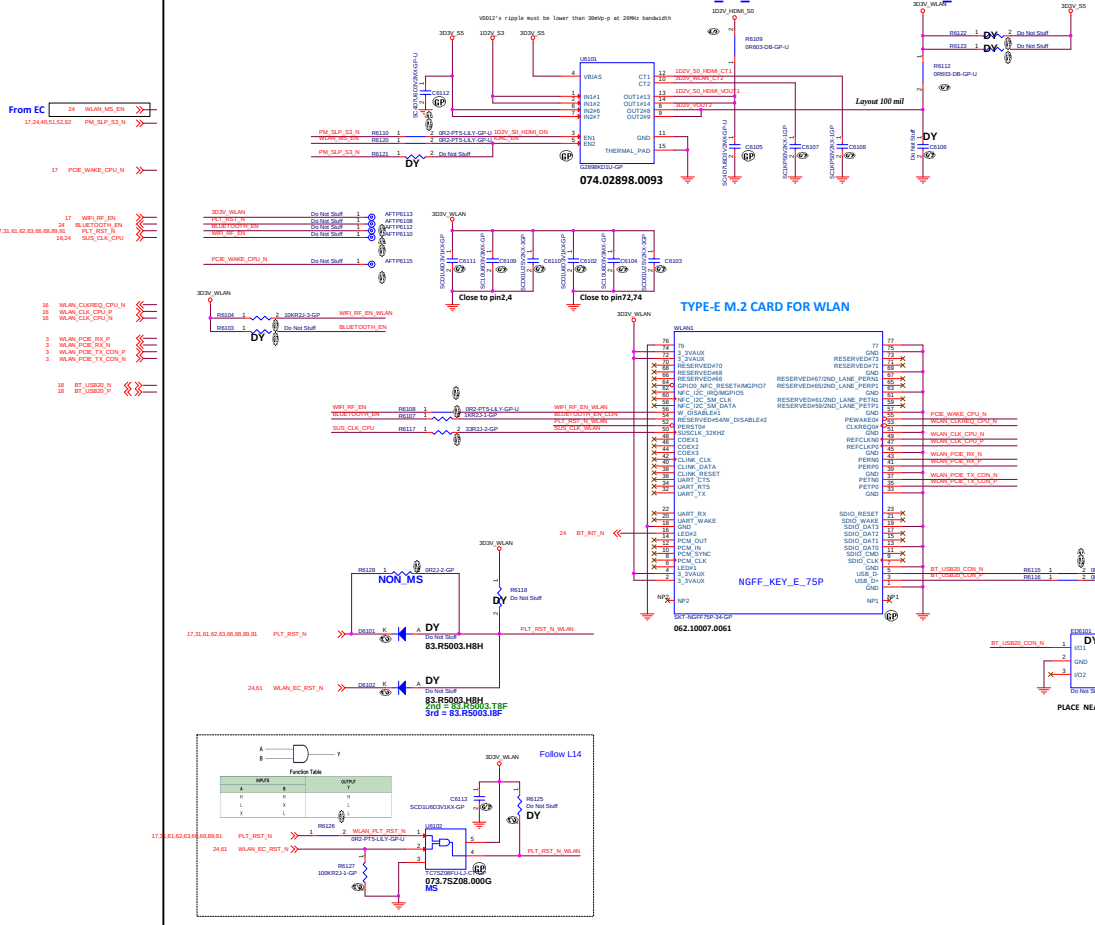

Table 3–1 Key AE 2230-platform and module pinout (M.2 revision fo

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	Voltage on Card Side	WLAN or BT
1	GND	GND		
2	3.3 V	3.3 V	3.3 V	All
3	USB_D+	USB_D+	3.3 V	BT
4	3.3 V	3.3 V	3.3 V	All
5	USB_D-	USB_D-	3.3 V	BT
6	LED1	LED1	3.3v	WLAN
7	GND	GND		
8	Connector key	Connector key		
9	Connector key	Connector key		
10	Connector key	Connector key		
11	Connector key	Connector key		
12	Connector key	Connector key		
13	Connector key	Connector key		
14	Connector key	Connector key		
15	Connector key	Connector key		
16	LED2	LED2	3.3v	BT
17	NC	NC	NA	
18	GND	GND		
19	NC	NC	NA	
20	NC	NC	NA	
21	NC	NC	NA	
22	NC	NC	NA	
23	NC	NC	NA	
24	Connector Key	Connector Key		
25	Connector Key	Connector Key		

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	Voltage on Card Side	WLAN or BT
26	Connector Key	Connector Key		
27	Connector Key	Connector Key		
28	Connector Key	Connector Key		
29	Connector Key	Connector Key		
30	Connector Key	Connector Key		
31	Connector Key	Connector Key		
32	NC	NC	NA	
33	GND	GND		
34	NC	NC	NA	
35	PETp0	PERp0	PCIe PHY	WLAN
36	NC	NC	NA	
37	PETn0	PERn0	PCIe PHY	WLAN
38	CLINK RESET (O)(0/3.3 V)	CLINK RESET (I)(0/3.3 V)	3.3 V	WLAN
39	GND	GND		
40	CLINK DATA	CLINK DATA	CLINK PHY (1 V)	WLAN
41	PERp0	PETp0	PCIe PHY	WLAN
42	CLINK CLK	CLINK CLK	CLINK PHY (1 V)	WLAN
43	PERn0	PETn0	PCIe PHY	WLAN
44	COEX3(I/O) (0/1.8V)	COEX3(I/O) (0/1.8 V)	1.8 V	WLAN + BT
45	GND	GND		
46	COEX2(I/O) (0/1.8V)	COEX2(I/O)(0/1.8V)	1.8 V	WLAN + BT
47	REFCLKP0	REFCLKP0	PCIe PHY	WLAN
48	COEX1 (I/O)(0/1.8 V)	COEX1 (I/O)(0/1.8V)	1.8 V	WLAN + BT

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	Voltage on Card Side	WLAN or BT
49	REFCLKN0	REFCLKN0	PCIe PHY	WLAN
50	SUSCLK (32 kHz) (O)(0/3.3 V)	SUSCLK (32 kHz) (I)(0/3.3 V)	3.3 V	WLAN + BT
51	GND	GND		
52	PERST0# (O)(0/3.3 V)	PERST0# (I)(0/3.3 V)	3.3 V	WLAN
53	CLKREQ0# (IO)(0/3.3 V)	CLKREQ0# (IO)(0/3.3 V)	3.3 V	WLAN
54	W_DISABLE2# (O)(0/3.3 V)	W_DISABLE2# (I)(0/3.3 V)	3.3 V	BT
55	PEWAKE0# (IO)(0/3.3 V)	PEWAKE0# (IO)(0/3.3 V)	3.3 V	WLAN
56	W_DISABLE1# (O)(0/3.3 V)	W_DISABLE1# (I)(0/3.3 V	3.3v	WLAN
57	GND	GND		
58	I2C DATA (IO)(UART_RX (I)(0/1.8)	I2C DATA (IO)(UART_TX (O)(0/1.8 V)	1.8 V	WLAN + BT
59	PETp1	PERp1	PCIe PHY	N/A
60	I2C CLK/UART_TX (O)(0/1.8 V)	I2C CLK/UART_RX (I)(0/1.8 V)	1.8 V	WLAN + BT
61	PETn1	PERn1	PCIe PHY	N/A
62	ALERT#/UART_CTS (I)(0/1.8 V)	ALERT#/UART_RTS (O)(0/1.8 V)	1.8 V	WLAN + BT
63	GND	GND		

Pin #	Pin Name Platform Pinout	Pin Name Module Pinout	Voltage on Card Side	WLAN or BT
64	NFC_RESET#/UART_RTS (O)(0/1.8 V)	NFC_RESET#/UART_CTS (I)(0/1.8 V)	1.8 V	WLAN + BT
65	PERp1	PETp1	PCIe PHY	N/A
66	PERST1# (O)(0/3.3 V)	PERST1# (I)(0/3.3 V)	3.3 V	N/A
67	PERn1	PETn1	PCIe PHY	N/A
68	CLKREQ1# (IO)(0/3.3 V)	CLKREQ1# (IO)(0/3.3 V)	3.3 V	N/A
69	GND	GND		
70	PEWAKE1# (IO)(0/3.3 V)	PEWAKE1# (IO)(0/3.3 V)	3.3 V	N/A
71	REFCLKP1	REFCLKP1	PCIe PHY	N/A
72	3.3 V	3.3 V		
73	REFCLKN1	REFCLKN1	PCIe PHY	N/A
74	3.3 V	3.3 V		
75	GND	GND		

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Title: INT IO (WLAN M.2)

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Date: Wednesday, April 06, 2022 | Sheet 61 of 105

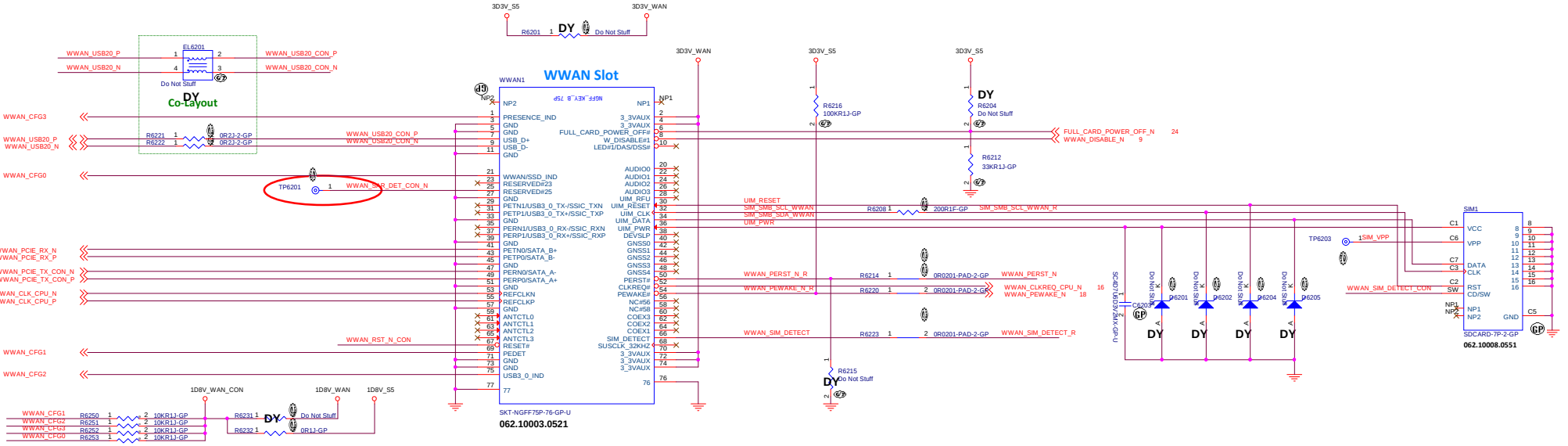
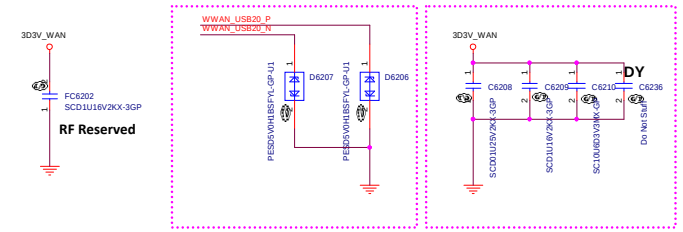
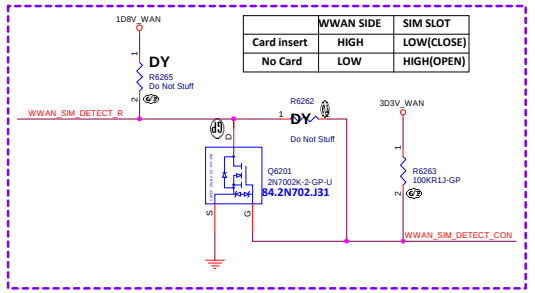
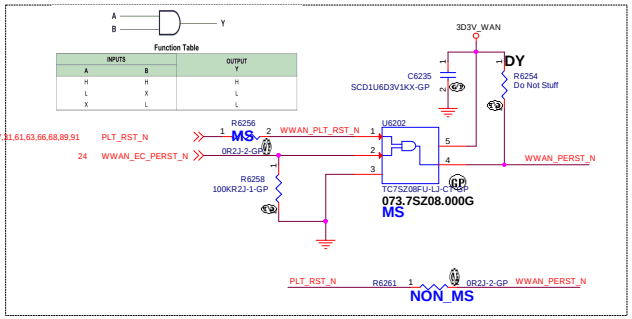


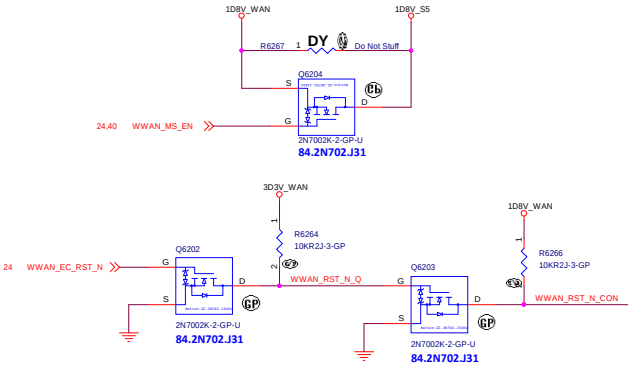
TABLE:

State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	GND	GND	NC	SSD - PCIe	N/A
2	GND	GND	NC	GND	WWAN - PCIe	0
3	GND	GND	NC	NC	WWAN - PCIe	1
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3
8	NC	GND	GND	GND	WWAN - SSIC	0
9	NC	GND	GND	NC	WWAN - SSIC	1
10	NC	GND	NC	GND	WWAN - SSIC	2
11	NC	GND	NC	NC	WWAN - SSIC	3
12	NC	NC	GND	GND	WWAN - PCIe	2
13	NC	NC	GND	NC	WWAN - PCIe	3
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined
15	NC	NC	NC	NC	No Module Present	N/A

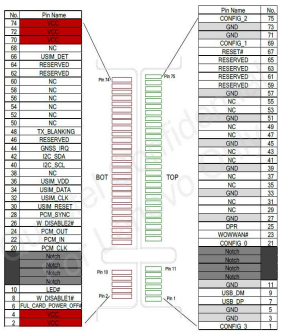








The following figure shows the pin assignment of EM05-XX.



The L860 module applies standard M.2 Key-B interface, with a total of 75 pins.

3.1.1 Pin Map

L14 L15 LAN

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Title: INT IO (WWAN/PCIE RE-DRIVER)

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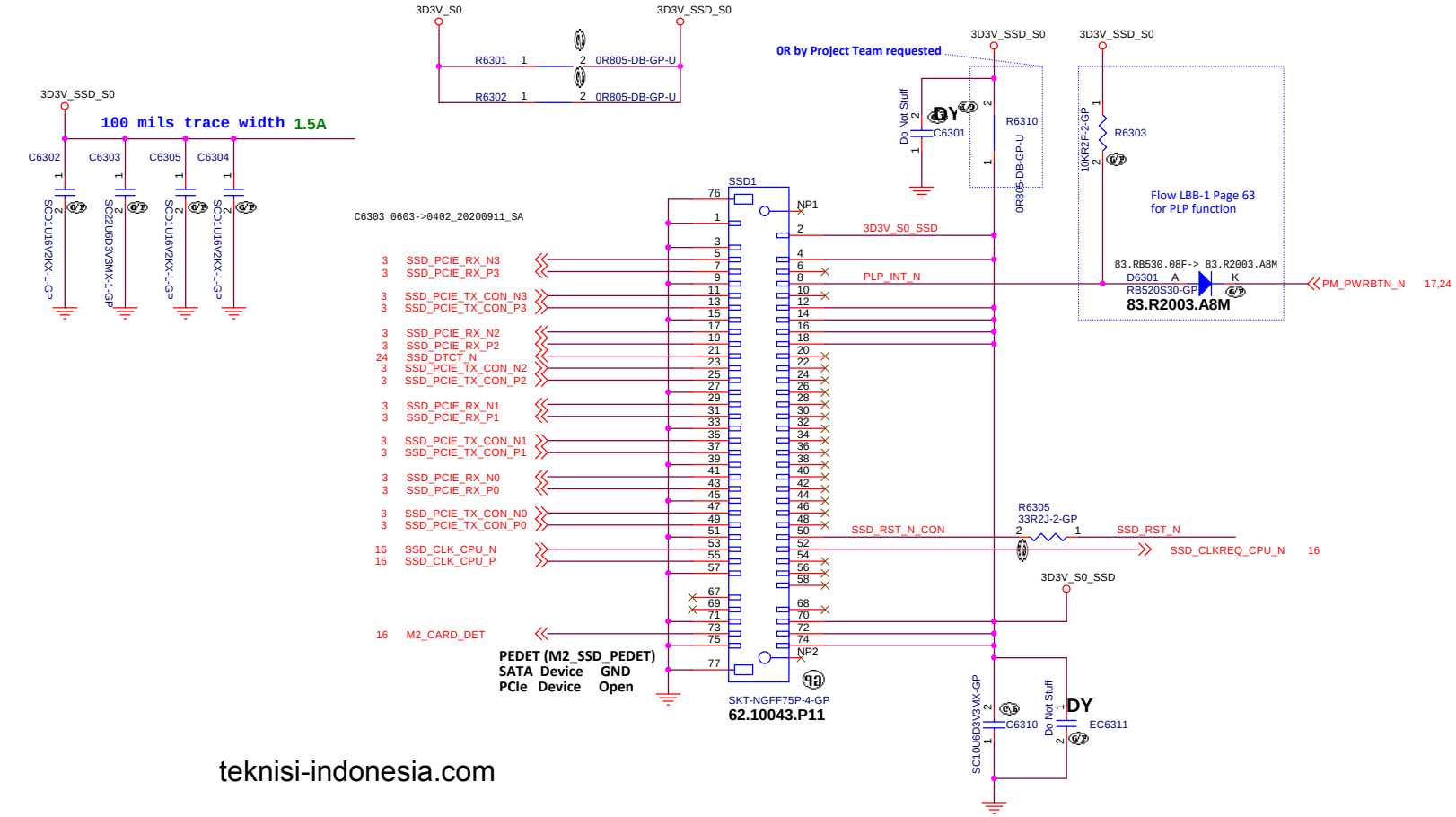
Date: Wednesday, April 06, 2022 | Sheet 62 of 106

NGFF Connector

TYPE-M M.2 CARD FOR SSD



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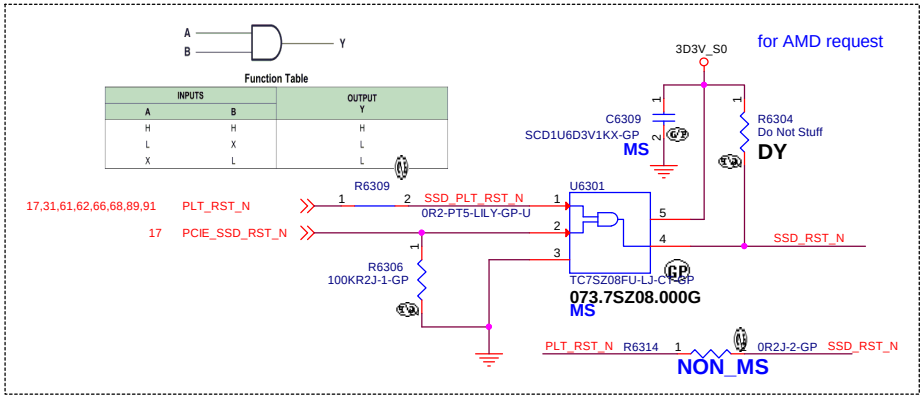

5.3. SSD Socket; Socket 3 (Mechanical Key M)

This Socket pinout and key are only intended for SSD devices. The Host I/Fs supported are PCIe with up to four lanes or SATA. The state of the PEDET pin (69) will indicate to the platform which I/F of these two is actually connected.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	

5.2 Pin Assignments

[Table 11] Pin Assignments

PIN#(Top)	Description	PIN#(Bottom)	Description
1	GND	2	3.3V
3	GND	4	3.3V
5	PERn3	6	NC
7	PERp3	8	PLN#
9	GND	10	DAS#
11	PETn3	12	3.3V
13	PETp3	14	3.3V
15	GND	16	3.3V
17	PERn2	18	3.3V
19	PERp2	20	NC
21	GND	22	NC
23	PETn2	24	NC
25	PETp2	26	NC
27	GND	28	NC
29	PERn1	30	NC
31	PERp1	32	NC
33	GND	34	NC
35	PETn1	36	NC
37	PETp1	38	NC
39	GND	40	SMB_SCL
41	PERn0	42	SMB_SDA
43	PERp0	44	SMB_ALERT#
AM630 Product Specification			
RPITJ256MGE1QDQ / RPITJ512MGE1QDQ / RPETJ256MGE2MDQ / RPETJ512MGE2QDQ / RPETJT24MGE2QDQ			
45	GND	46	NC
47	PETn0	48	NC
49	PETp0	50	PERST#
51	GND	52	CLKREQ#
53	REFCLKN	54	NC
55	REFCLKP	56	UART_TX
57	GND	58	UART_RX
	Module Key		Module Key
	Module Key		Module Key
	Module Key		Module Key
	Module Key		Module Key
67	NC	68	NC
69	NC	70	3.3V
71	GND	72	3.3V
73	GND	74	3.3V
75	GND		

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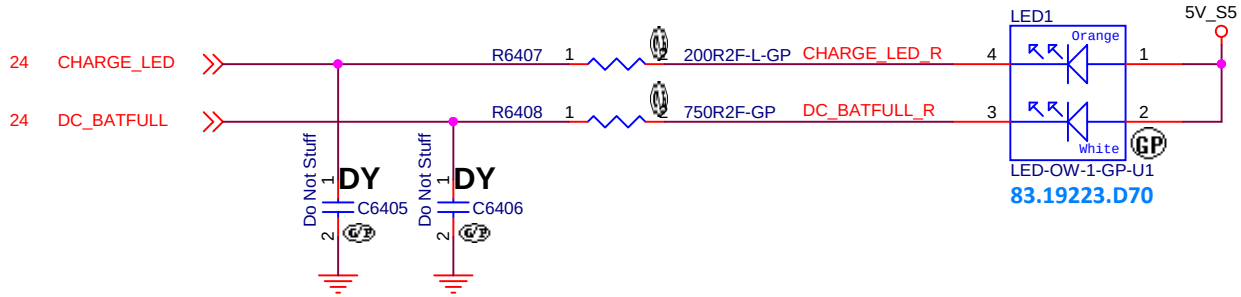
Title: INT IO (SSD M.2/ eMMC)

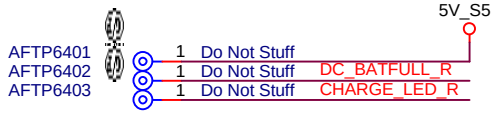
Size: A3 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 63 of 106

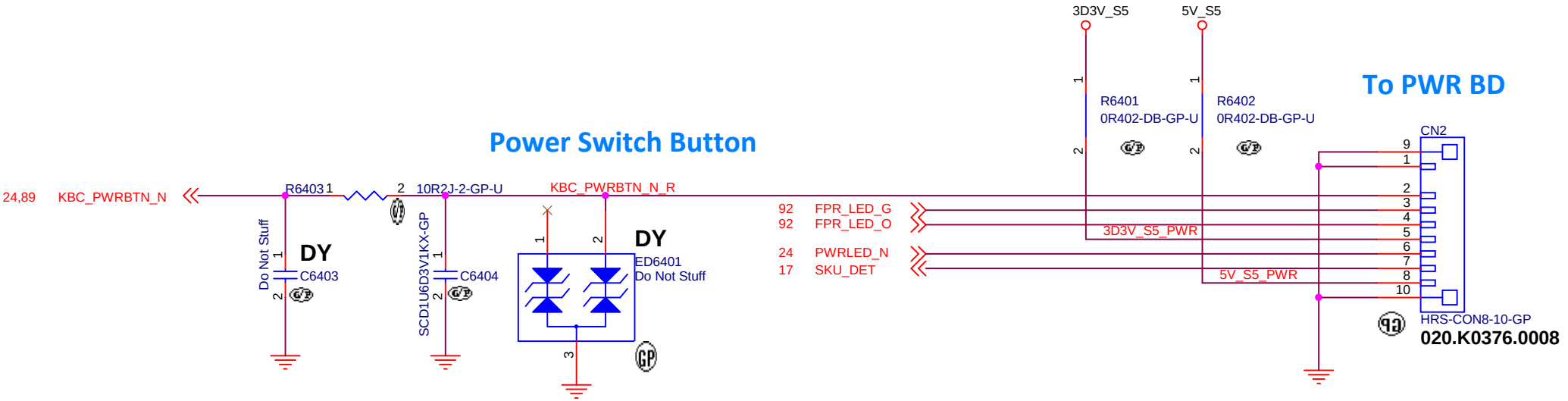
Charger Dual LED



Near LED1



Power Switch Button



L14 L15 LAN

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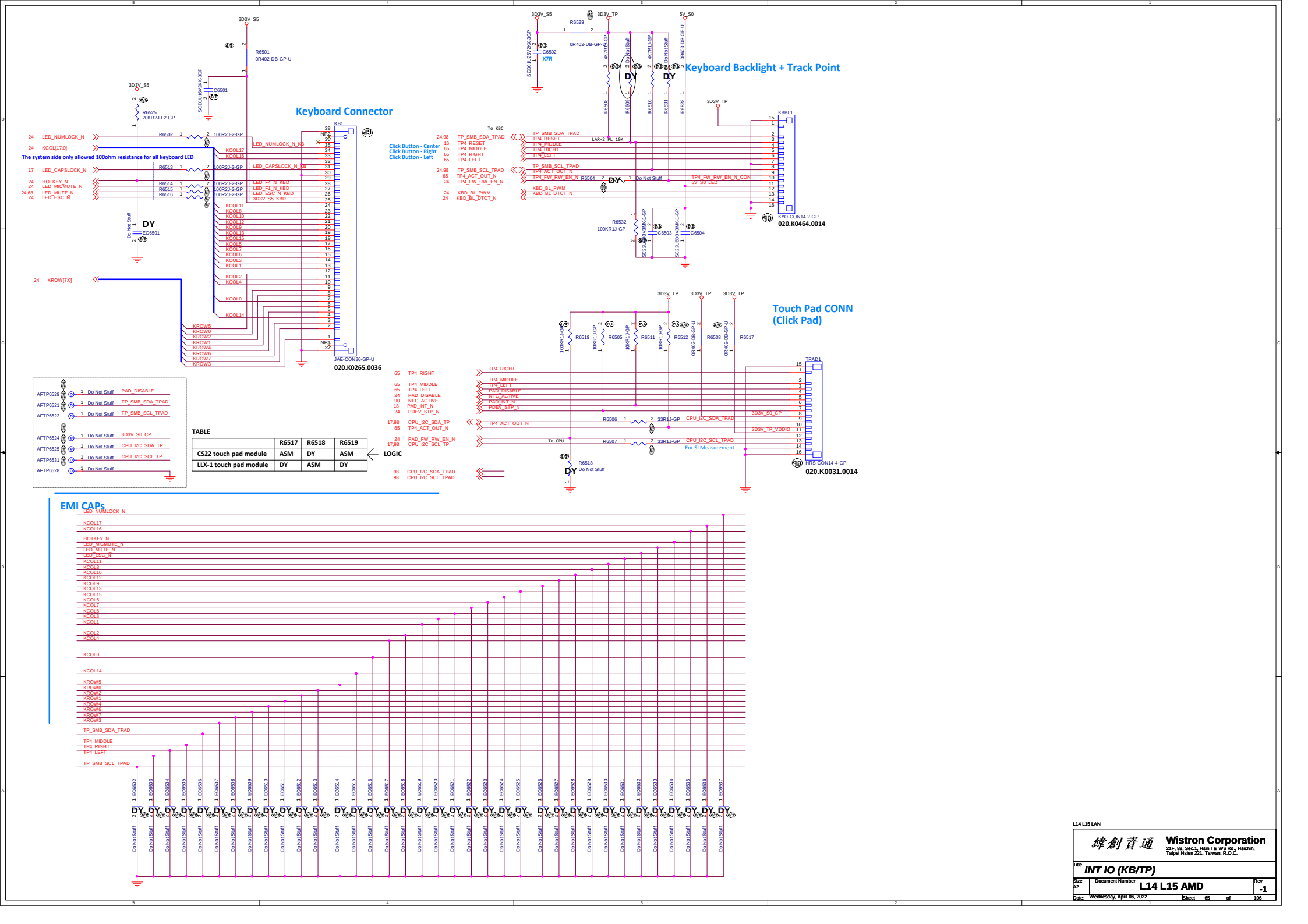
Title: LED / BUTTON / POWER BUTTON		
Size: A4	Document Number: L14 L15 AMD	Rev: -1
Date: Wednesday, April 06, 2022	Sheet 64 of 106	



	R6517	R6518	R6519
CS22 touch pad module	ASM	DY	ASM
LLX-1 touch pad module	DY	ASM	DY

L14 L15 LAN

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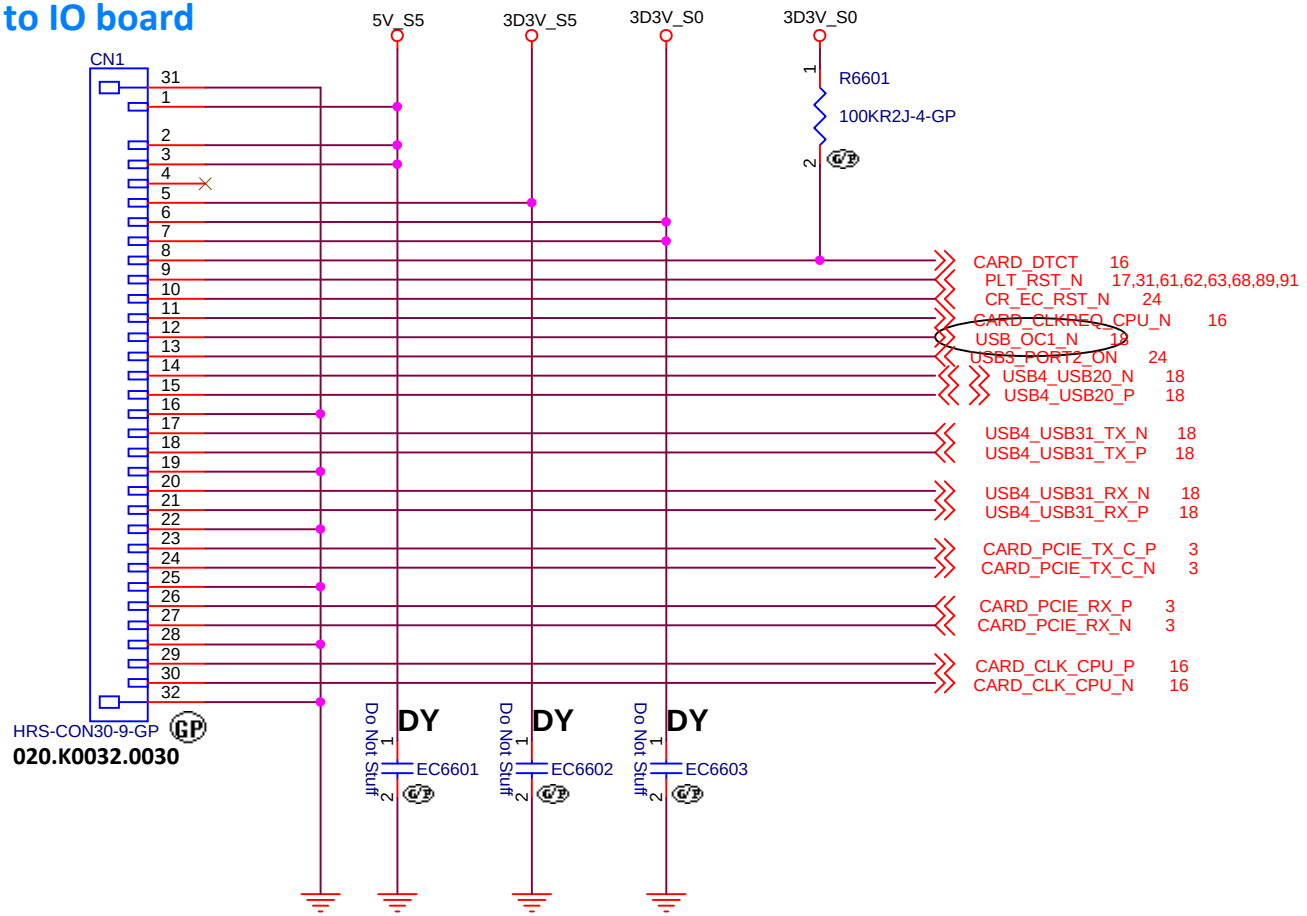
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/TP)

Size: A2 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 65 of 106

MB to IO board



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Title: *IO BOARD CONN (SNBD/WFCAM)*		
Size: A4	Document Number: **L14 L15 AMD**	Rev: **-1**
Date: Wednesday, April 06, 2022	Sheet 66 of 106	

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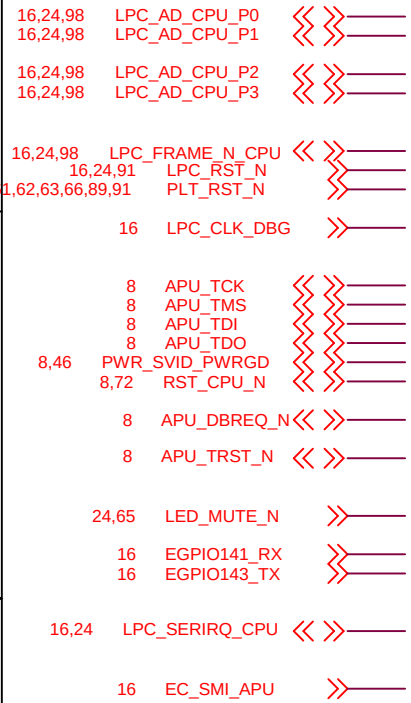
Title ***SENSOR (RSVD)***

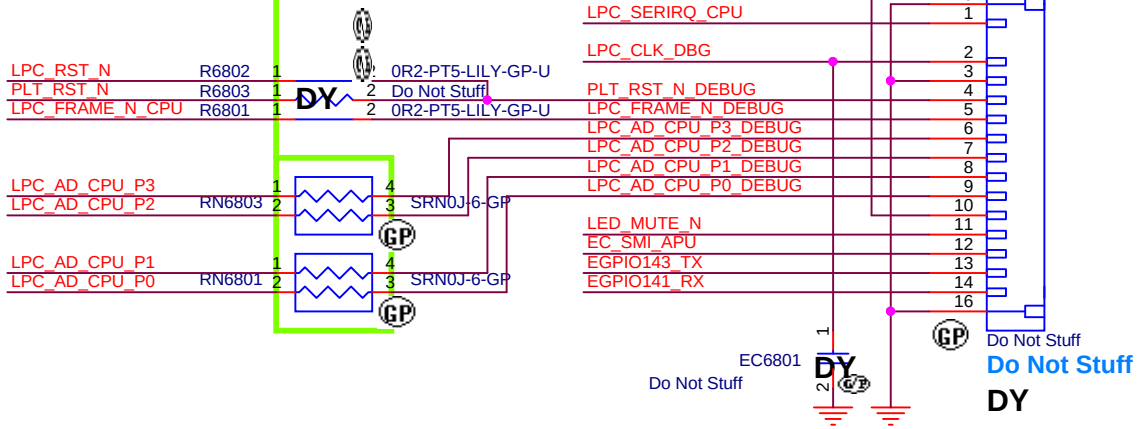
Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 67 of 106

Debug Connector



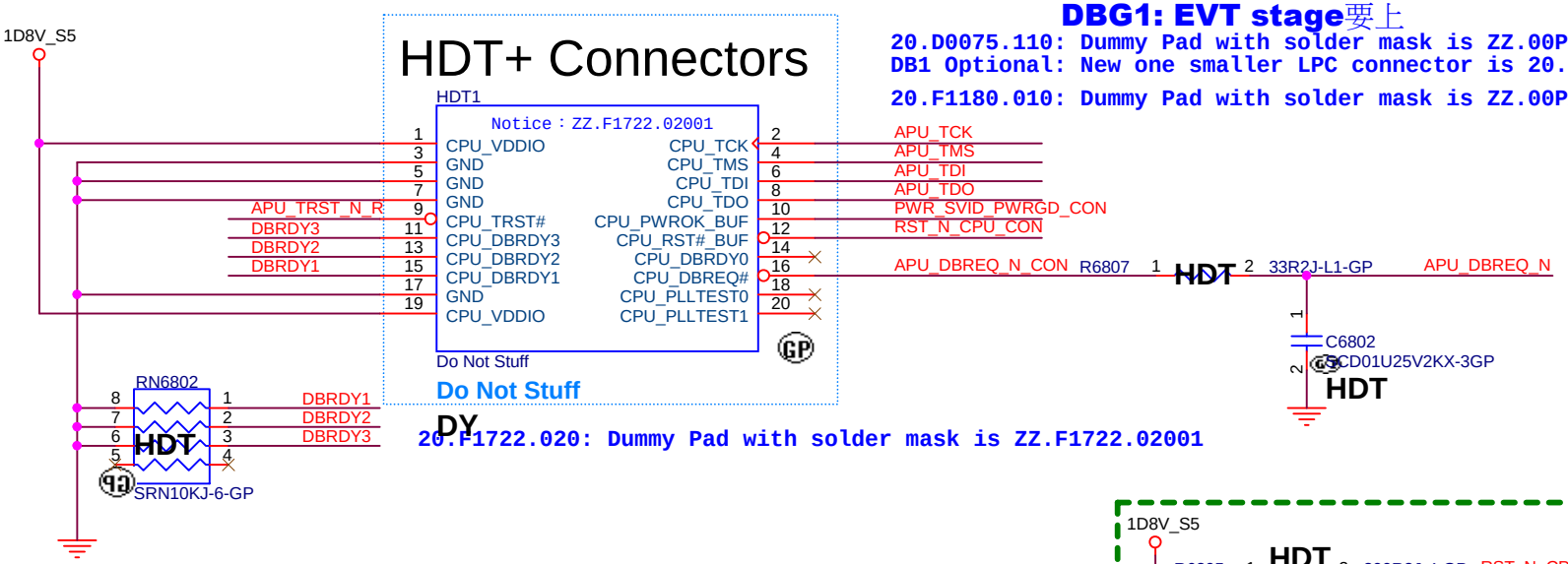
Layout Note:
Place near trace separated point.



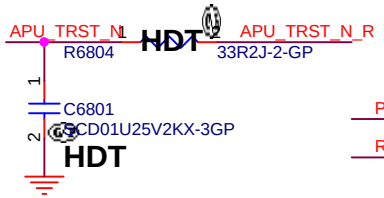
DBG1: EVT stage要上

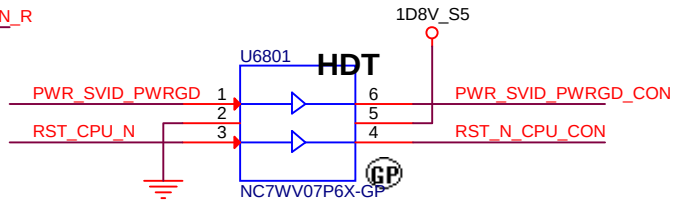
20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.
20.F1180.010: Dummy Pad with solder mask is ZZ.00PAD.GV1

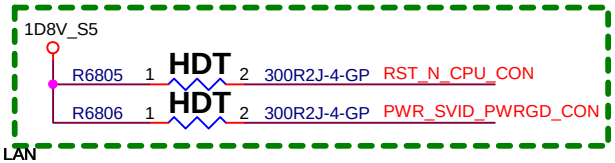
HDT+ Connectors



20.F1722.020: Dummy Pad with solder mask is ZZ.F1722.02001







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Title	**DEBUG (LPC/HDT)**	
Size A4	Document Number **L14 L15 AMD**	Rev **-1**
Date: Wednesday, April 06, 2022	Sheet 68 of 106	

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L14 L15 LAN

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Title ***SENSOR (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 69 of 106

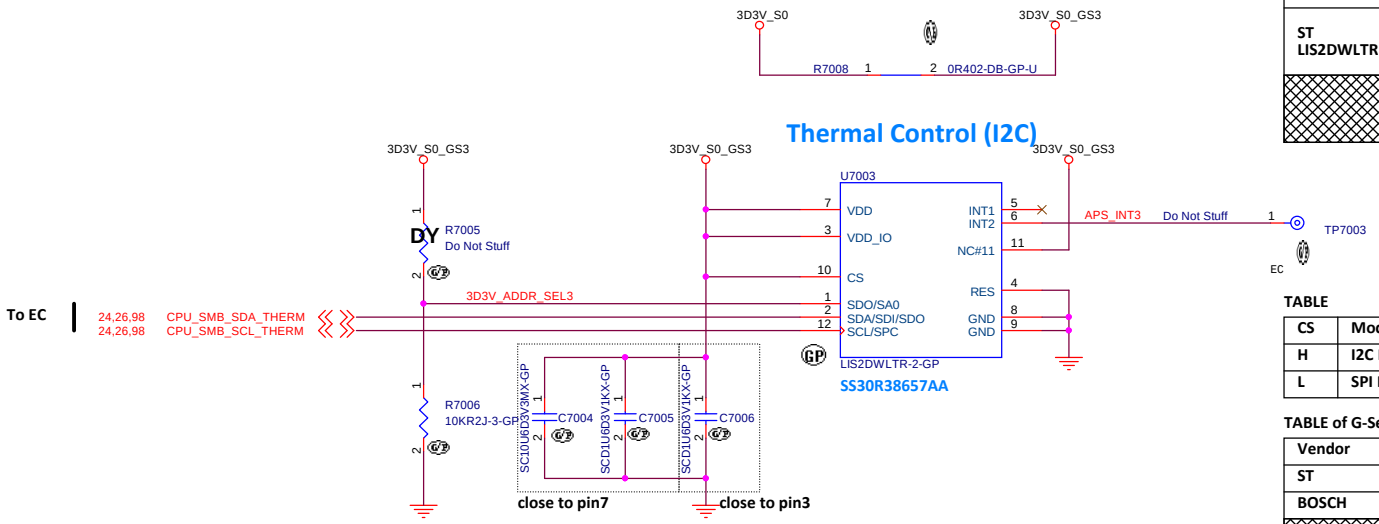

TABLE for ITS Detection (U7003): Tri-axis Digital Accelerometer

P/N	ADDR_SEL3	Address (8bit)	
ST LIS2DWLTR	H	32h (W) & 33h (R)	← LOGIC
	L	30h (W) & 31h (R)	

TABLE

CS	Mode Selection	
H	I2C Mode	← LOGIC
L	SPI Mode	

TABLE of G-Sensor (U7003)

Vendor	P/N	Wistron P/N	DS P/N	
ST	LIS2DWLTR	074.LIS2D.00B0	SS30R38657AA	
BOSCH	BMA422	074.00422.M003	SS31E39793AA	
~~BOSCH~~	~~BMA280~~	~~074.00280.0A00~~	~~SS30R37529AA~~	Use it at EC side only
		074.00422.00B0		

CHG U7003 BOSCH source from BMA280 (EOL) to BMA422

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Title: ***SENSOR (G-SENSOR)***

Size	Document Number	Rev
A3	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 70 of 106

BLANK

L14 L15 LAN

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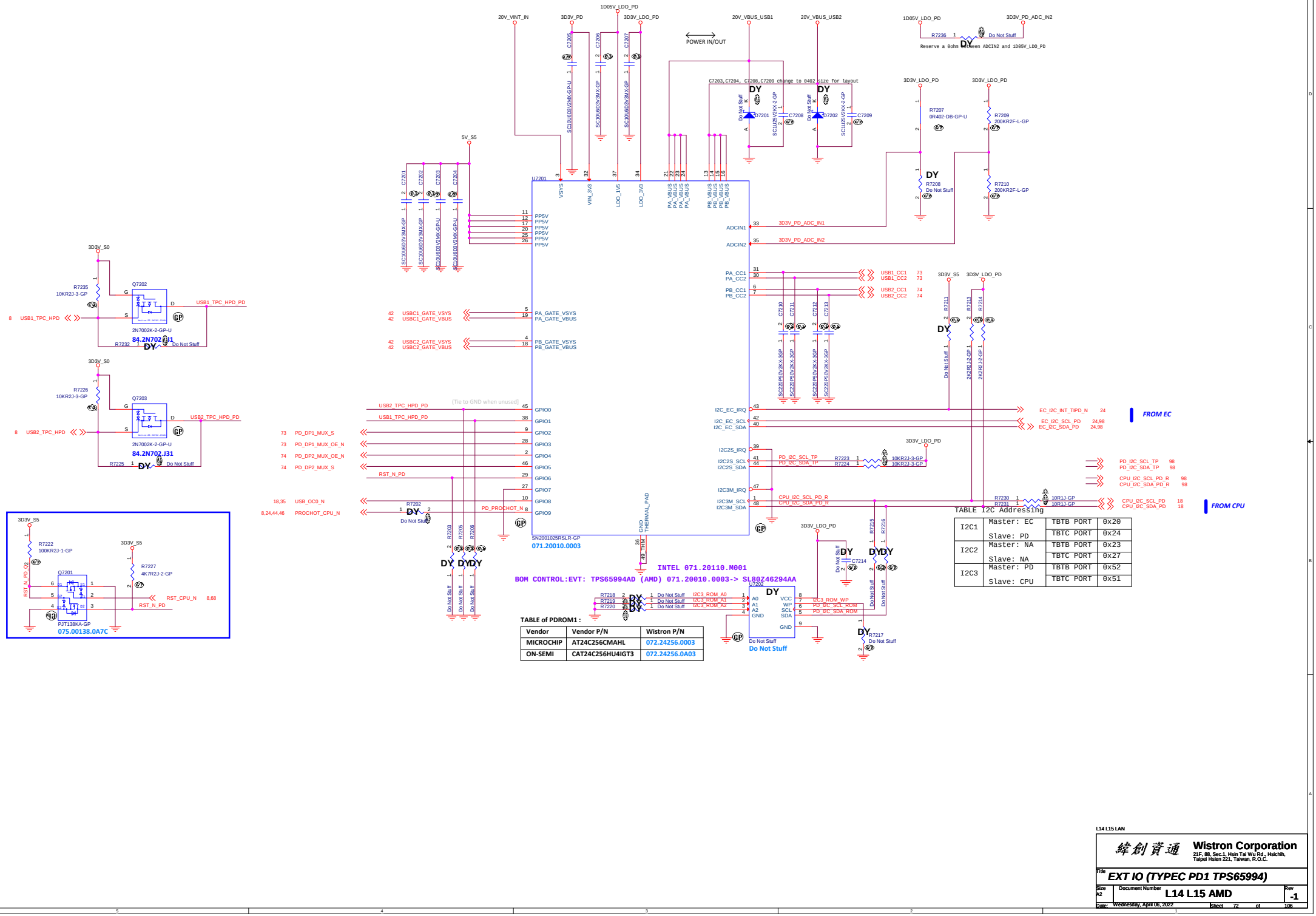
Title ***EXT IO (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 71 of 106


20V_VINT_IN
3D3V_PD
1D05V_LDO_PD
3D3V_LDO_PD
POWER IN/OUT
20V_VBUS_USB1
20V_VBUS_USB2
3D3V_PD_ADC_IN2
Reserve a 0ohm between ADCIN2 and 1D05V_LDO_PD
C7203,C7204, C1208,C7209 change to 0402 size for layout
5V_S5
U7201
SN2001025RSLR-GP
071.20010.0003
INTEL 071.20110.M001
BOM CONTROL:EVT: TPS65994AD (AMD) 071.20010.0003-> SL80Z46294AA
3D3V_S0
3D3V_S5
Q7202
Q7203
Q7201
2N7002K-2-GP-U
84.2N702.J31
PJT138KA-GP
075.00138.0A7C
USB1_TPC_HPD_PD
USB2_TPC_HPD_PD
RST_N_PD_Q2
RST_CPU_N
RST_N_PD
USB_OC0_N
PROCHOT_CPU_N
PD_DP1_MUX_S
PD_DP1_MUX_OE_N
PD_DP2_MUX_OE_N
PD_DP2_MUX_S
USBC1_GATE_VSYS
USBC1_GATE_VBUS
USBC2_GATE_VSYS
USBC2_GATE_VBUS
PA_GATE_VSYS
PA_GATE_VBUS
PB_GATE_VSYS
PB_GATE_VBUS
PA_CC1
PA_CC2
PB_CC1
PB_CC2
USB1_CC1
USB1_CC2
USB2_CC1
USB2_CC2
I2C_EC_IRQ
I2C_EC_SCL
I2C_EC_SDA
I2C2S_IRQ
I2C2S_SCL
I2C2S_SDA
I2C3M_IRQ
I2C3M_SCL
I2C3M_SDA
EC_I2C_INT_TIPD_N
EC_I2C_SCL_PD
EC_I2C_SDA_PD
PD_I2C_SCL_TP
PD_I2C_SDA_TP
CPU_I2C_SCL_PD_R
CPU_I2C_SDA_PD_R
CPU_I2C_SCL_PD
CPU_I2C_SDA_PD
FROM EC
FROM CPU
(Tie to GND when unused)
Do Not Stuff
DY
TABLE I2C Addressing
TABLE of PDROM1 :
Vendor | Vendor P/N | Wistron P/N
MICROCHIP | AT24C256CMAHL | 072.24256.0003
ON-SEMI | CAT24C256HU4IGT3 | 072.24256.0A03
I2C1 | Master: EC / Slave: PD | TBTB PORT | 0x20 / TBTC PORT | 0x24
I2C2 | Master: NA / Slave: NA | TBTB PORT | 0x23 / TBTC PORT | 0x27
I2C3 | Master: PD / Slave: CPU | TBTB PORT | 0x52 / TBTC PORT | 0x51
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Title: EXT IO (TYPEC PD1 TPS65994)
Size: A2
Document Number: L14 L15 AMD
Rev: -1
Date: Wednesday, April 06, 2022
Sheet 72 of 106

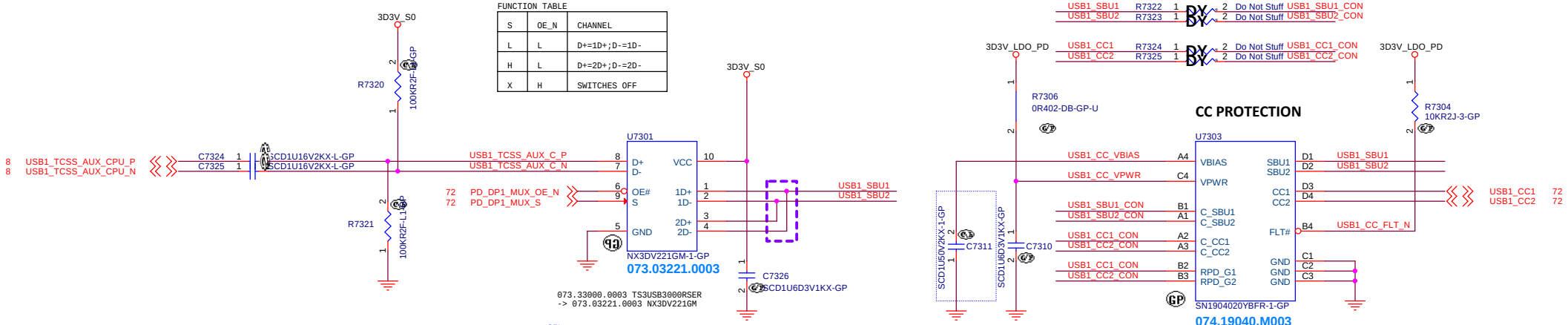
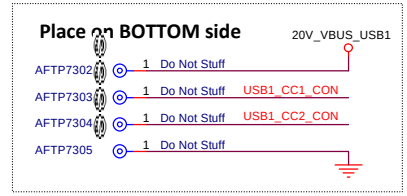
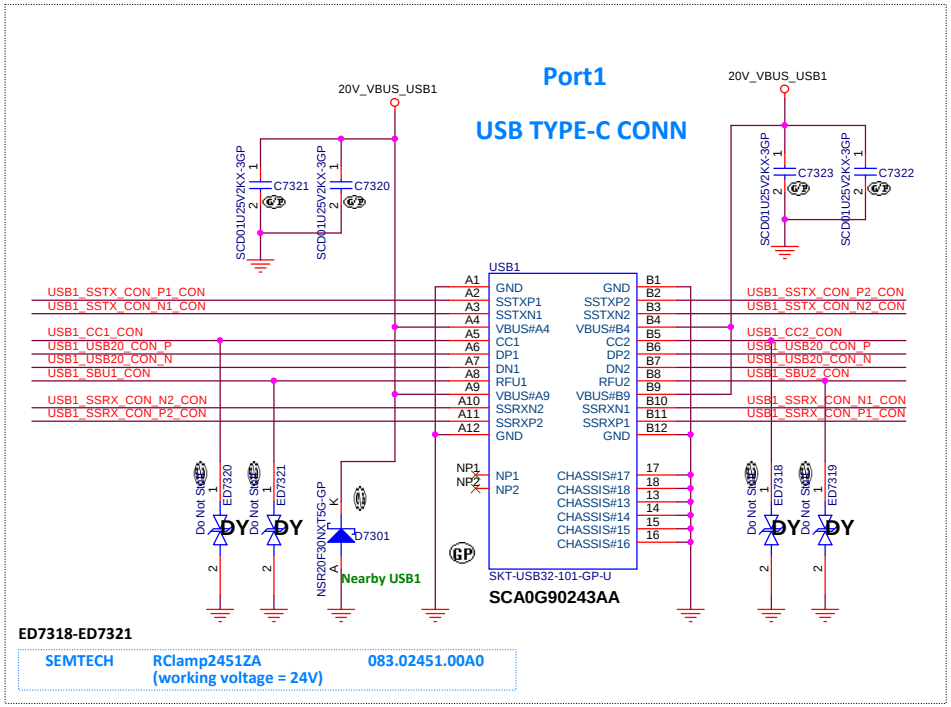
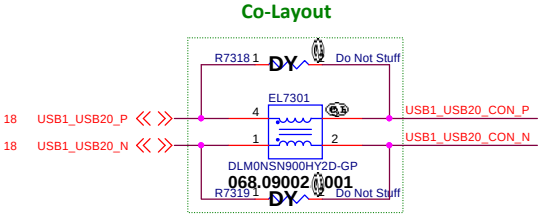


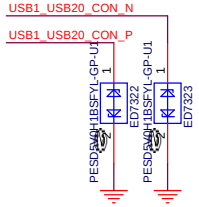
TABLE of U7303

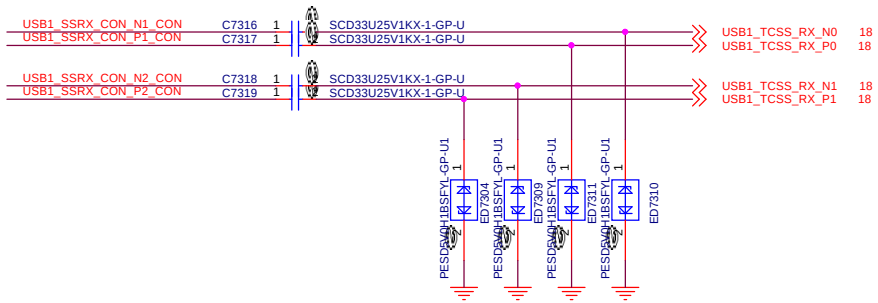
Vendor	Vendor P/N	Wistron P/N	DS P/N	
TI	SN1904020YBFR	074.19040.M003	SL80W65004AA	
KINETIC	KTU1121AEGAB-TA	074.01121.0A7Z	SL81G98087AA	KTU1121EGAB-TA 074.01121.007Z for TNB
RICHTEK	LVJ1701WSC	074.01701.M001	SL81G98088AA	
TI	SN1904020AYBFR	074.19040.M004	SL81F38020AA	
RICHTEK	RT1738CWSC	074.01738.009Z	SL81H36416	for LNB
RICHTEK	RT1738AGQW(Z0B)	074.01738.0093	SL81E60983	

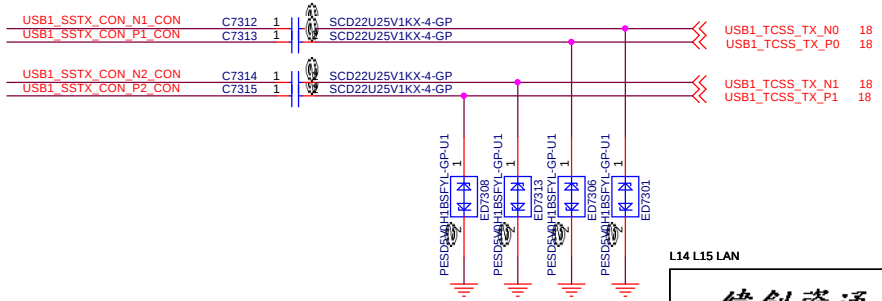












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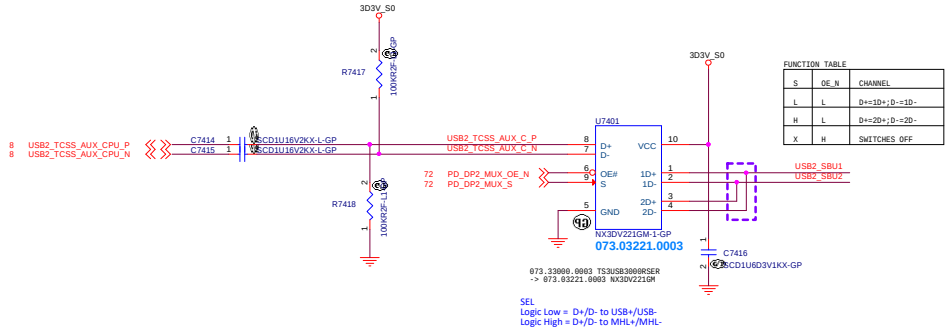
Title: EXT IO (TYPEC CONN/PROTECT)

Size: A3 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 73 of 106



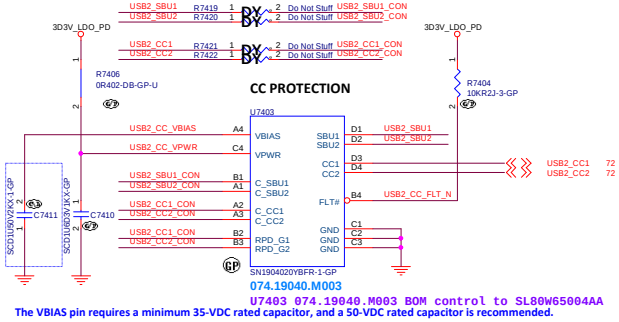
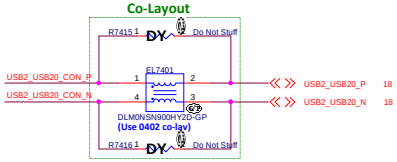
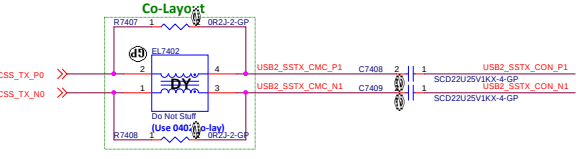
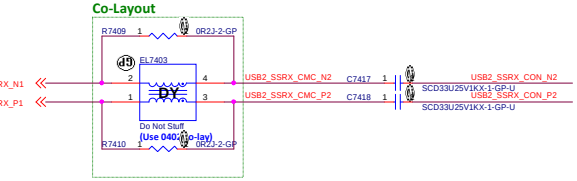


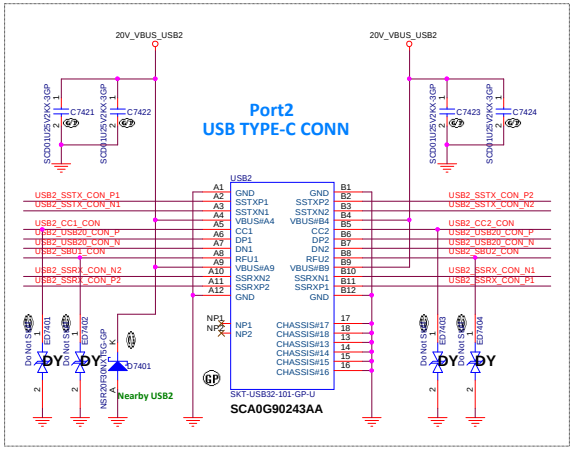
TABLE of U7403

Vendor	Vendor P/N	Wistron P/N	DS P/N	
TI	SN1904020YBFR	074.19040.M003	SL80W65004AA	
KINETIC	KTU1121AEGAB-TA	074.01121.0A7Z	SL81G98087AA	074.01121.007Z
RICHTEK	LVJ1701WSC	074.01701.M001	SL81G98088AA	
TI	SN1904020AYBFR	074.19040.M004	SL81F38020AA	
RICHTEK	RT1738CWSC	074.01738.009Z	LVJ1710(=RT1738C)	



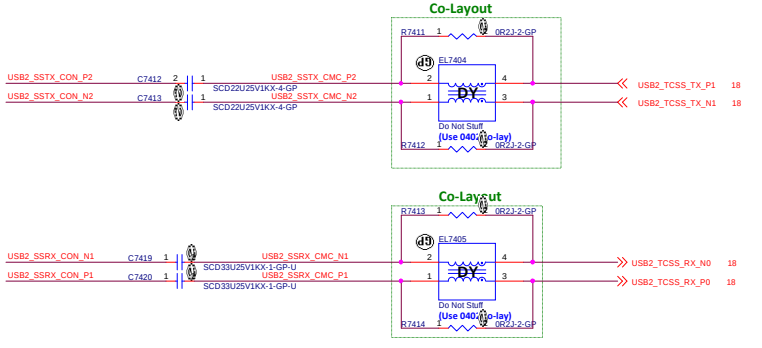


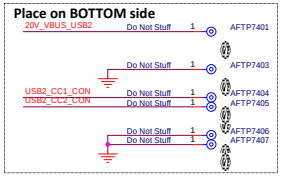


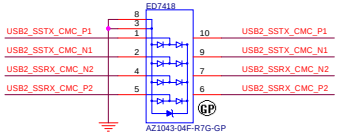


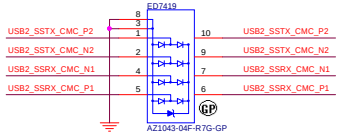
ED7401-ED7404

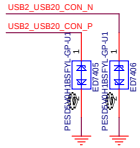
SEMTECH	RClamp2451ZA (working voltage = 24V)	083.02451.00A0











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Title: EXT IO (TYPEC CONN/PROTECT)

Size	Document Number	Rev
A2	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 74 of 106

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L14 L15 LAN

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Title: ***EXT IO***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 75 of 106

BLANK

L14 L15 LAN

緯創資通 **Wistron Corporation**
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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 76 of 106

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L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 77 of 106

BLANK

L14 L15 LAN

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU (RSVD)**

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 78 of 106

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Title: ***GPU (RSVD)***		
Size: A4	Document Number: **L14 L15 AMD**	Rev: **-1**
Date: Wednesday, April 06, 2022	Sheet 79 of 106	

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L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 80 of 106

BLANK

L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 81 of 106

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L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 82 of 106

BLANK

L14 L15 LAN

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 83 of 106

BLANK

L14 L15 LAN

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 84 of 106

BLANK

L14 L15 LAN

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 85 of 106

BLANK

L14 L15 LAN

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Title: **GPU (RSVD)**

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 86 of 106

BLANK

L14 L15 LAN

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Title: *GPU (RSVD)*

Size	Document Number	Rev
A4	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 87 of 106

BLANK

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Title: ***GPU (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	-1

Date: Wednesday, April 06, 2022 Sheet 88 of 106

Spring Chip

SPR1
Do Not Stuff
Do Not Stuff
DY

Stand Off

HS1
STFT236B142R128H43-1-GP
34.4EO02.001

HS2
STF237R113H91-GP
434.0HH0K.0001

HS3
STF256R136-1H42-GP
434.0L802.0001

HS4
STFT236B142R128H43-1-GP
34.4EO02.001

PAD

H9
Do Not Stuff
Do Not Stuff

H10
Do Not Stuff
Do Not Stuff

H11
Do Not Stuff
Do Not Stuff

Test Point

TP8901
TP8903
Do Not Stuff
KBC_PWRBTN_N 24,64,89
Place on top side

TP8902
TP8904
Do Not Stuff
KBC_PWRBTN_N 24,64,89
Place on bottom side

AFTP8918
AFTP8921
Do Not Stuff
PLT_RST_N 17,31,61,62,63,66,68,91
KBC_PWRBTN_N 24,64,89
Place on top side

5V_S5 5V_S0 3D3V_S5 3D3V_S0

AFTP8901
AFTP8902
AFTP8903
AFTP8904
AFTP8905
AFTP8907
AFTP8908
AFTP8909
AFTP8910
AFTP8911
AFTP8912
Do Not Stuff

EMI CAPs

1D2V_S3: EC8901, EC8902, EC8903
19V_DCBATOUT: EC8906, EC8907, EC8908, EC8909, EC8910
3D3V_S0: EC8911, EC8912, EC8913
5V_S5: EC8915, EC8916, EC8917
3D3V_S0_SSD: EC8918
5V_S5_USB3: EC8920
3D3V_S5: EC8921, EC8922, EC8923

Do Not Stuff
DY

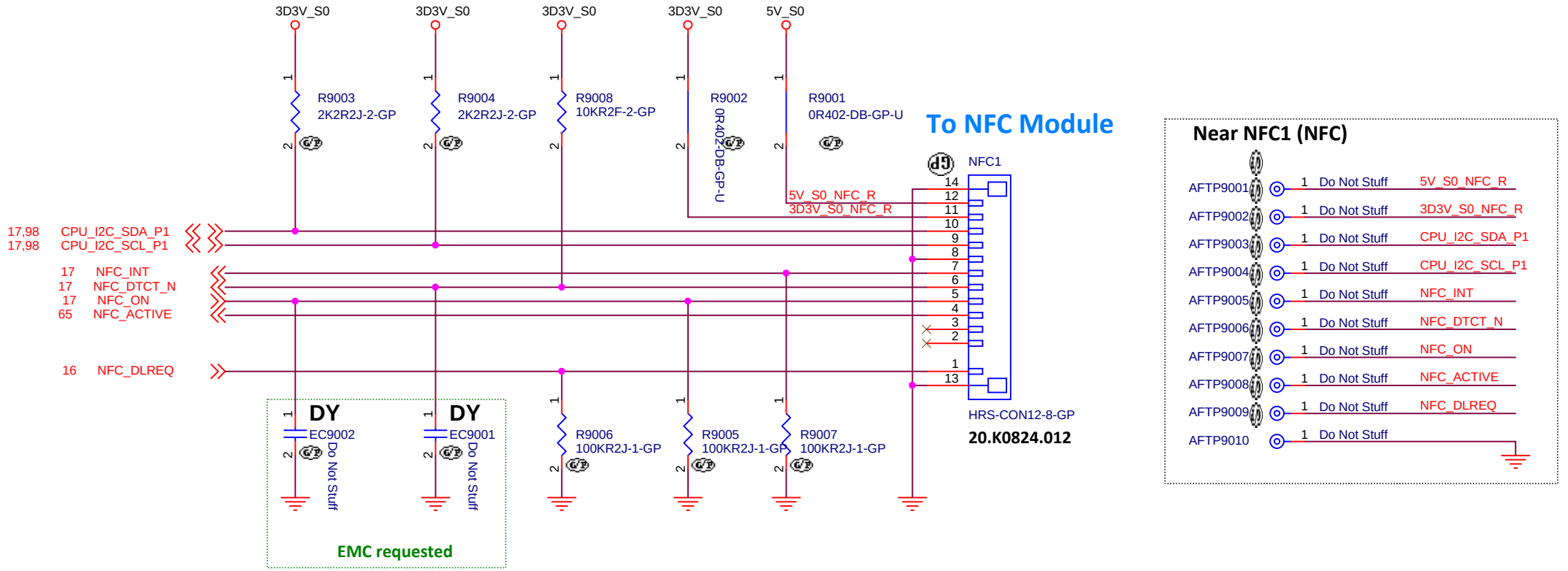
L14 L15 LAN

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS (ME/RF/EMI)***

Size	Document Number	Rev
A3	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 89 of 106



Pin	Symbol	Pin Type	Refer	Description
1	VBAT	Input Power	N/A	Power supply from system (4.5V - 5.5V)
2	PVDD	Input Power	N/A	Power supply to I/O (3.0V – 3.6V)
3	I2C_SDA	I/O	PVDD	I2C data
4	I2C _SCL	I	PVDD	I2C clock
5	GND	G	N/A	Ground
6	IRQ	O	PVDD	Interrupt from NFC module to the host (Host_Wake)
7	NFC_Presence	G	N/A	Connect to ground for NFC module presence bit (Low active)
8	VEN	I	VBAT	Reset pin. Set the device in Hard Power Down
9	TX_PWR_REQ	O	VDD	(External TX power supply request) (Active high 1.8V level output) Indicates NFC busy state during NFC communication to touchpad.
10	PMUVCC	Input Power	N/A	Power supply to UICC(1.78V~3.3V)
11	SWIO_UICC	I/O	VDD(SIM)	SWP data connection to SIM
12	DWL_REQ	I	PVDD	Firmware download control pin
S1	GND	G	N/A	Ground
S2	GND	G	N/A	Ground

Remark: P – power supply, G – ground, I – input, O – output, I/O – input/output

L14 L15 LAN

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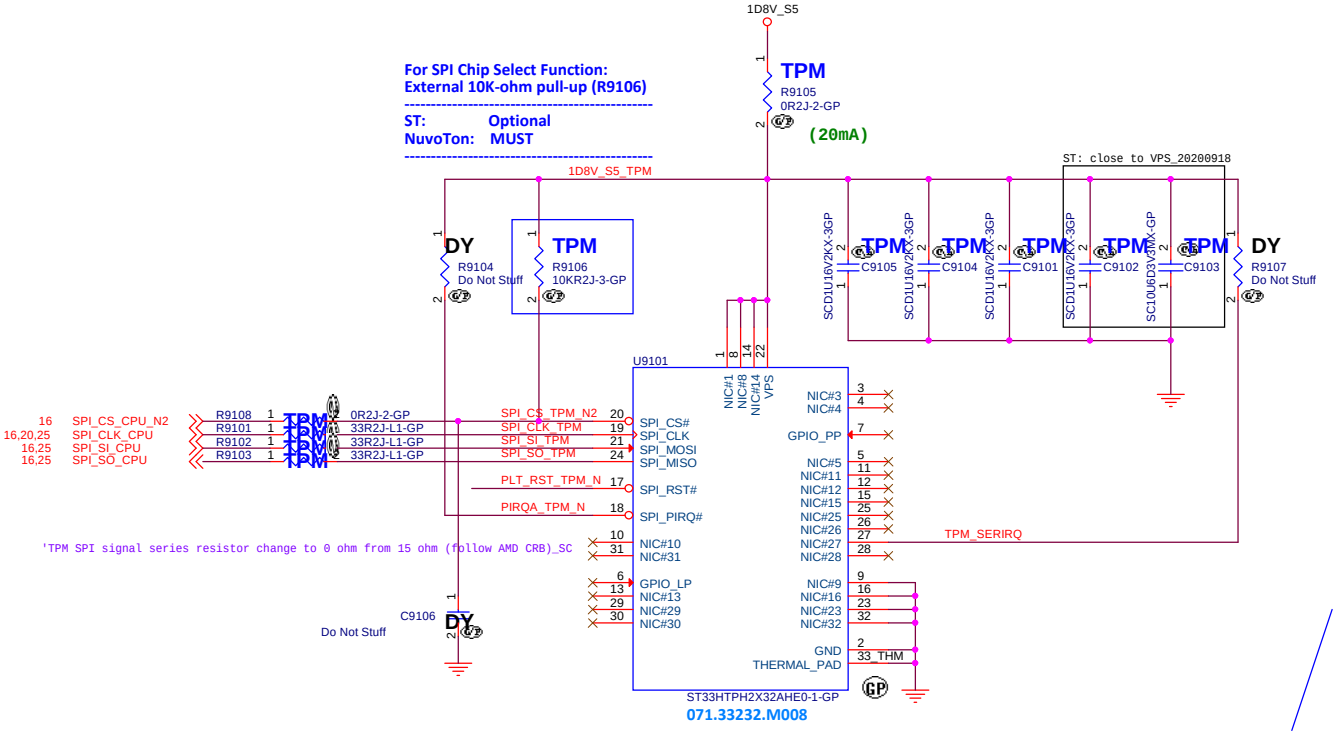
Title: ***INT IO (NFC)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	-1

Date: Wednesday, April 06, 2022 Sheet 90 of 106



SPI Chip Select Pin:
ST (SPI_CS#) Internal pull-up
NuvoTon (SCS#) Internal pull-up is disabled if the pin is part of the recognized host interface

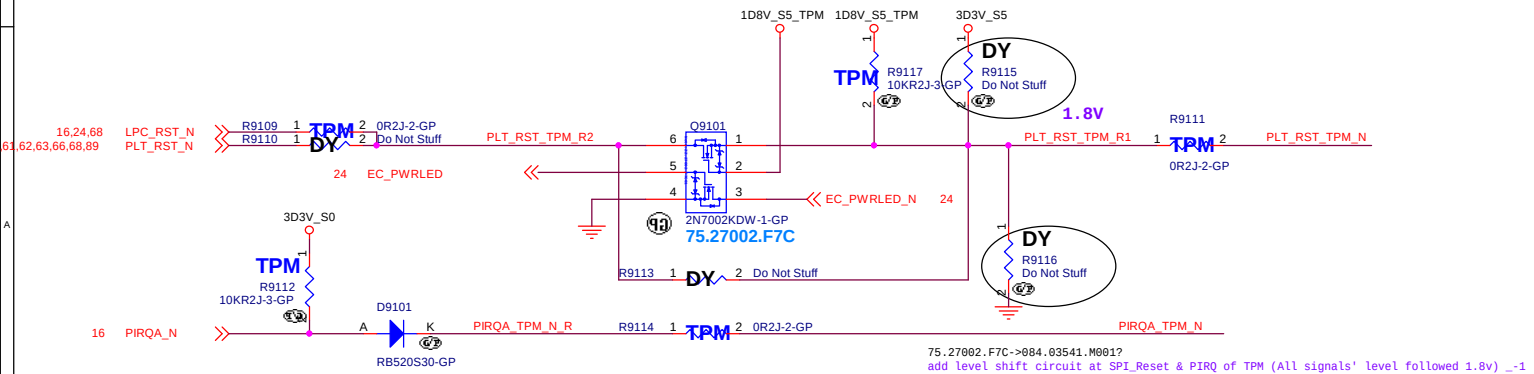
TABLE of U9101 : (TPM)

Vendor	Vendor P/N	Wistron P/N	DS P/N
ST Micro	ST33HTPH2X32AHE0	071.33232.M008	SL81D20418AA
Novoton	NPCT760LAAYX	071.00760.0A03	SL81D20417AA

TABLE of U9101 : (TCM)

Vendor	Vendor P/N	Wistron P/N	DS P/N
Nationz	Z32H330TC-SQN-L4	TBD	

Nationz:
Z32H330TC-SQN-L4 spec has not yet released



TABLE

Pin No	TCG PTP Spec(V38)	ST Micro ST33HTPH2X32AHE0	Novoton NPCT760LAAYX	Nationz Z32H330TC-SQN-L4
1	VDD	NC	VSB	VDD
2	GND	GND	NC	GND
3	NC	NC	NC	NC
4	GPIO	PP	GPIO/PP	NC
5	NC	NC	NC	NC
6	GPIO	NC	GPIO3	GPIO
7	GPIO	GPIO	NC	PP
8	VDD	NC	VHIO	VDD
9	NC	NC	NC	GND
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	NC	GPIO4	NC
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	NC
17	SPI_RST#	SPI_RST#	RST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5	CS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	NC	SDA/GPIO0	NC
30	SDA/GPIO0	NC	SCL/GPIO1	NC
31	NC	NC	NC	NC
32	NC	NC	NC	GND

TO BE UPDATE

L14 L15 LAN

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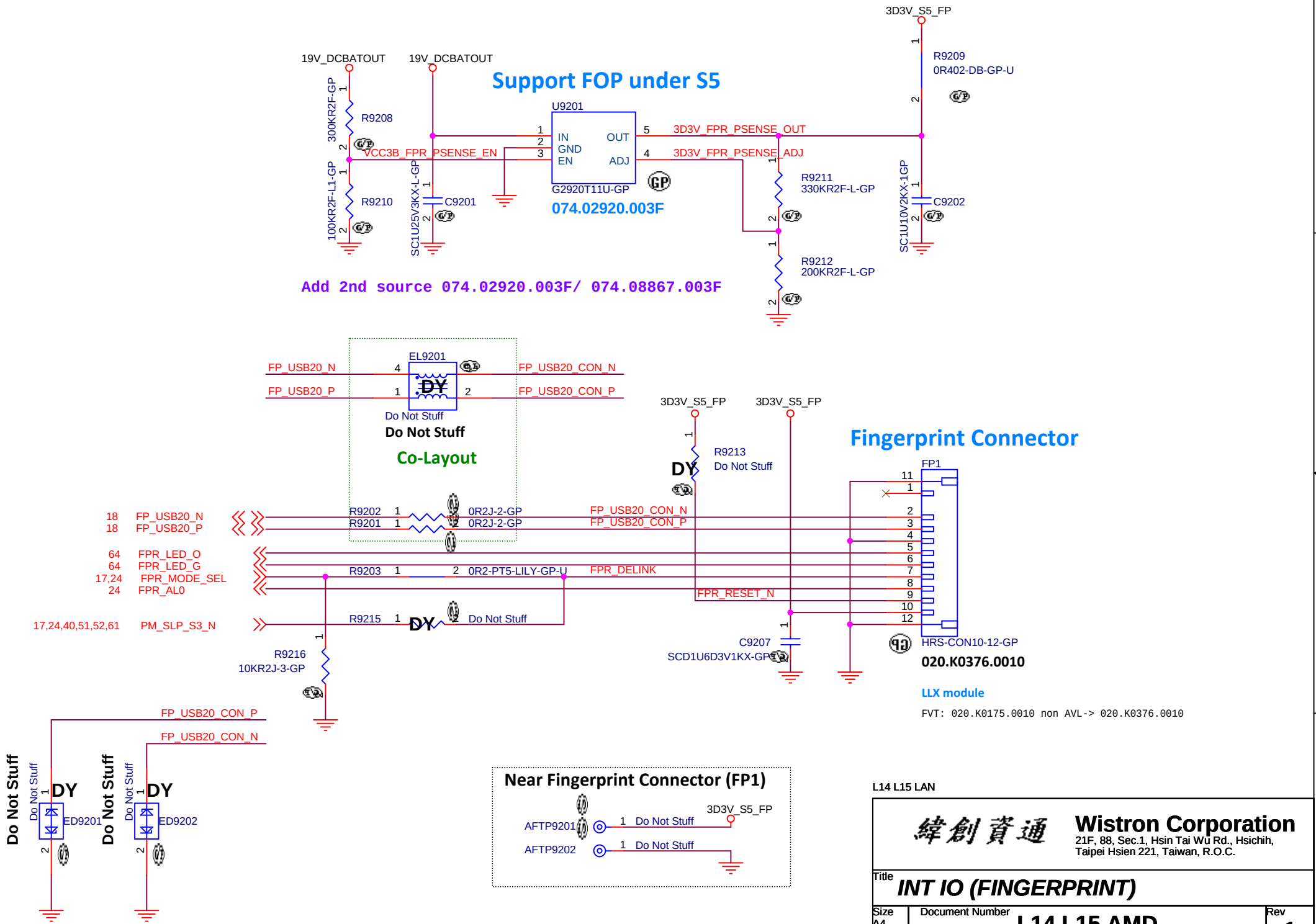
Title: INT IO (TPM 2.0)

Size: A3 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 91 of 106



L14 L15 LAN

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Title: ***INT IO (FINGERPRINT)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	-1
Date: Wednesday, April 06, 2022	Sheet 92 of 106	

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L14 L15 LAN

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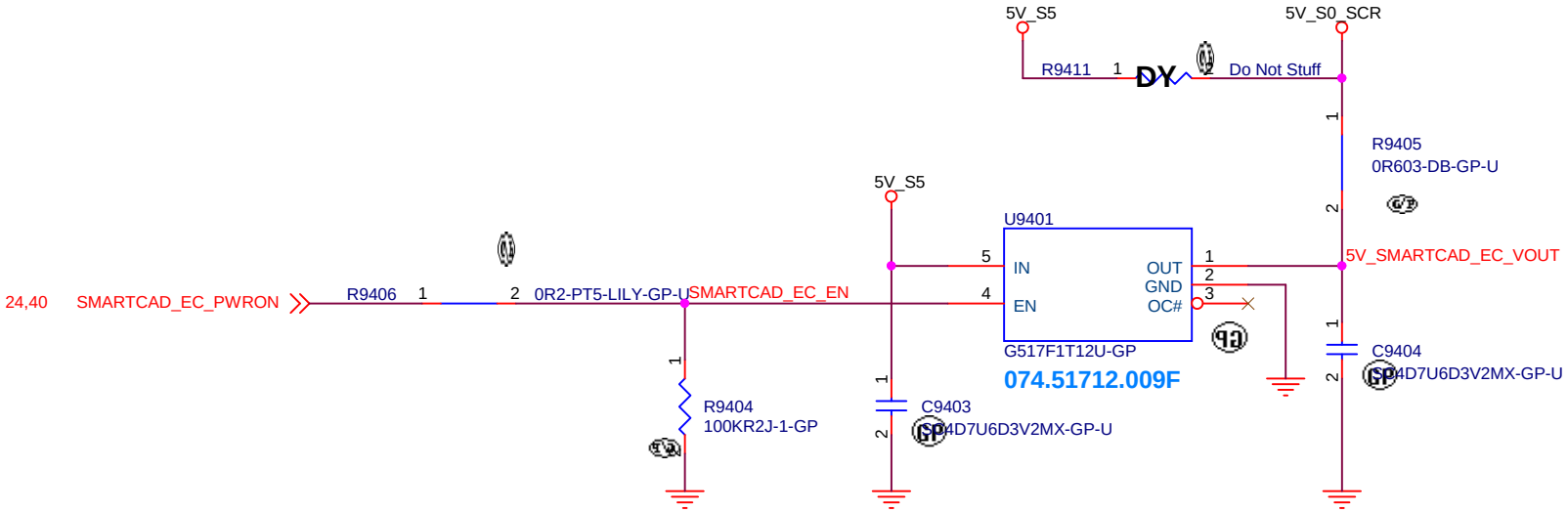
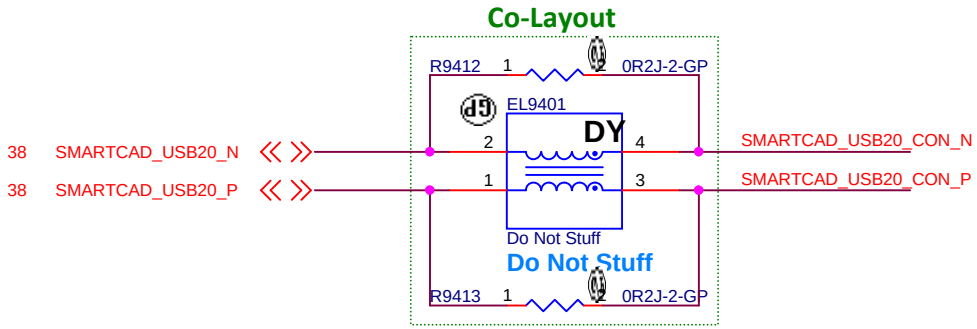
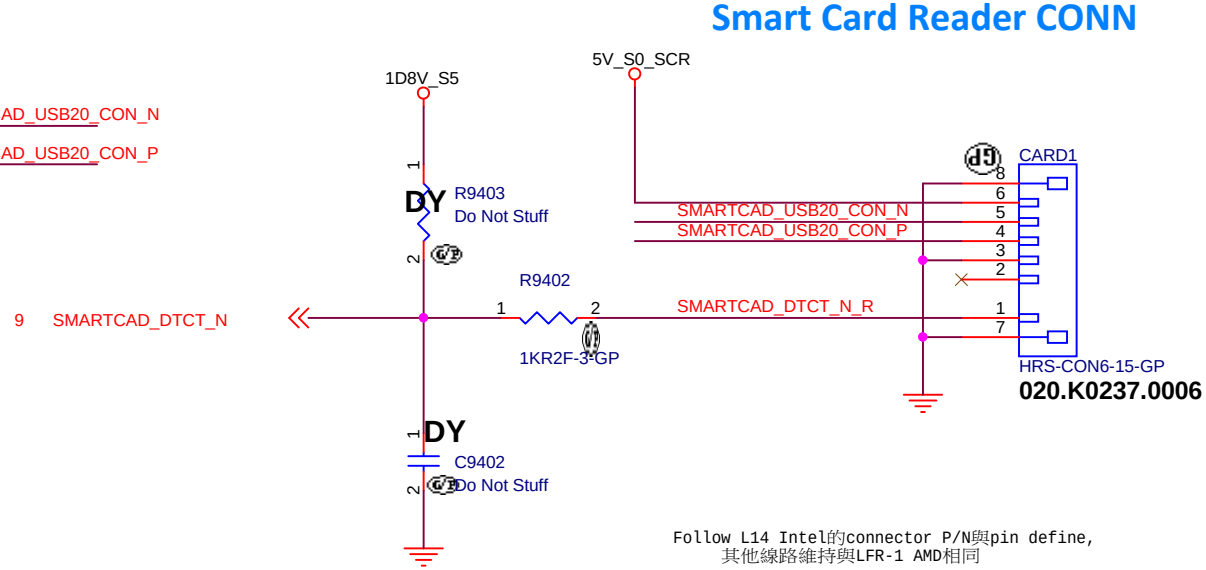
Title ***EXT IO (ACTIVE PEN)***

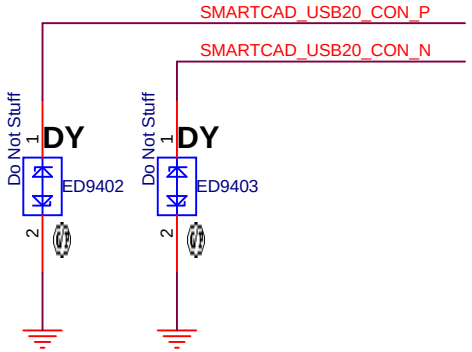
Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

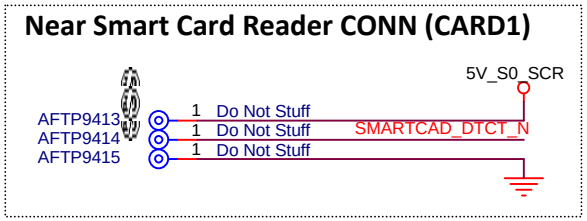
Date: Wednesday, April 06, 2022 Sheet 93 of 106











Follow L14 Intel的connector P/N與pin define,
其他線路維持與LFR-1 AMD相同

L14 L15 LAN

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Title **EXT IO (SMART CARD)**

Size	Document Number	Rev
A4	L14 L15 AMD	-1
Date: Wednesday, April 06, 2022	Sheet 94 of 106	

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L14 L15 LAN

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Title: ***EXT IO (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 95 of 106

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L14 L15 LAN

緯創資通 **Wistron Corporation**
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Title: ***COMMERCIAL (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 96 of 106

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L14 L15 LAN

緯創資通 **Wistron Corporation**
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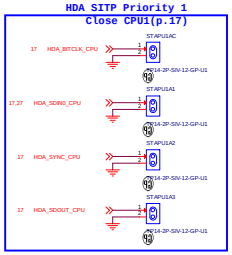
Title: ***COMMERCIAL (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 97 of 106

SITP DSN Template for 213005 LAR3 AMD(FENRIR-1)

HDA SITP Priority 1
Close CPU1(p.17)



HDA SITP Priority 1
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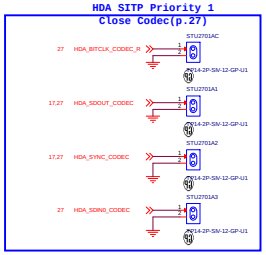

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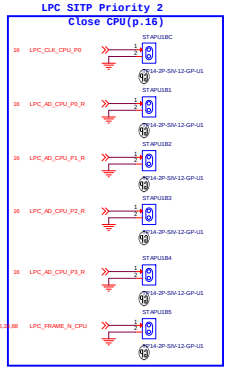

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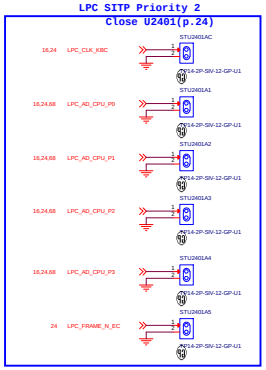
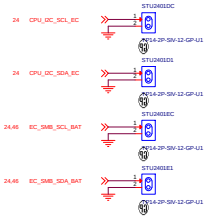
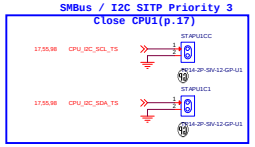




SMBus / I2C SITP Priority 3
Close CPU1(p.17)



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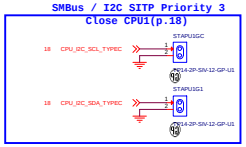
Close CPU1(p.18)



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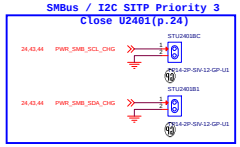

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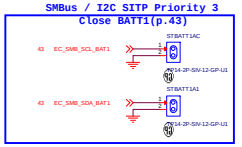
Close BATT1(p.43)



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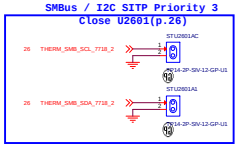

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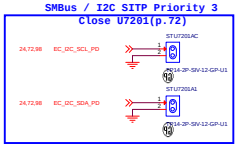

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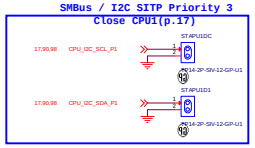

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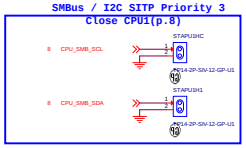

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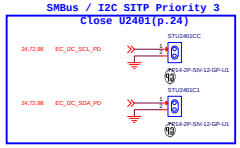

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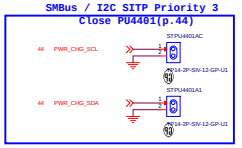

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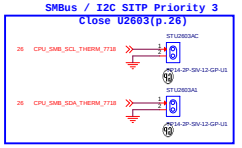

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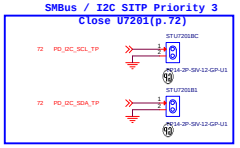

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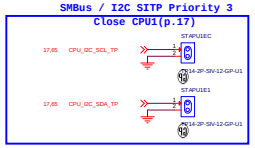

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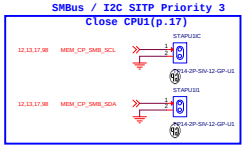
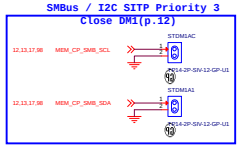


SMBus / I2C SITP Priority 3
Close DM1(p.12)



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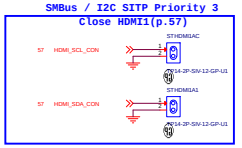

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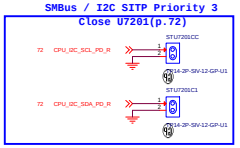
Close U7001(p.70)

SMBus / I2C SITP Priority 3
Close U7201(p.72)



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Close CPU1(p.17)

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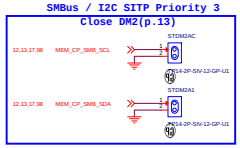

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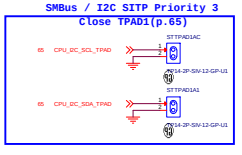

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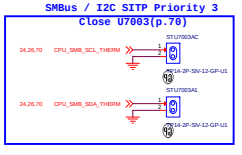

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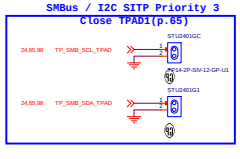

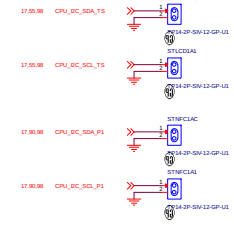

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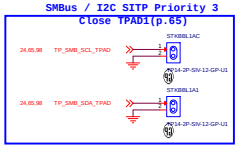

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Title: COMMERCIAL (SITP)

Size: A1 | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 04, 2007 | Sheet 98 of 105

BLANK

L14 L15 LAN

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Title: ***DEBUG (RSVD)***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 99 of 106

BLANK

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Title: ***TABLE OF CONTENT***

Size	Document Number	Rev
A4	**L14 L15 AMD**	**-1**

Date: Wednesday, April 06, 2022 Sheet 100 of 106

BLANK

L14 L15 LAN

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Title ***CHANGE HISTORY***

Size	Document Number	Rev
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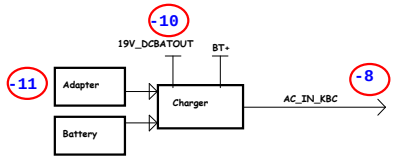
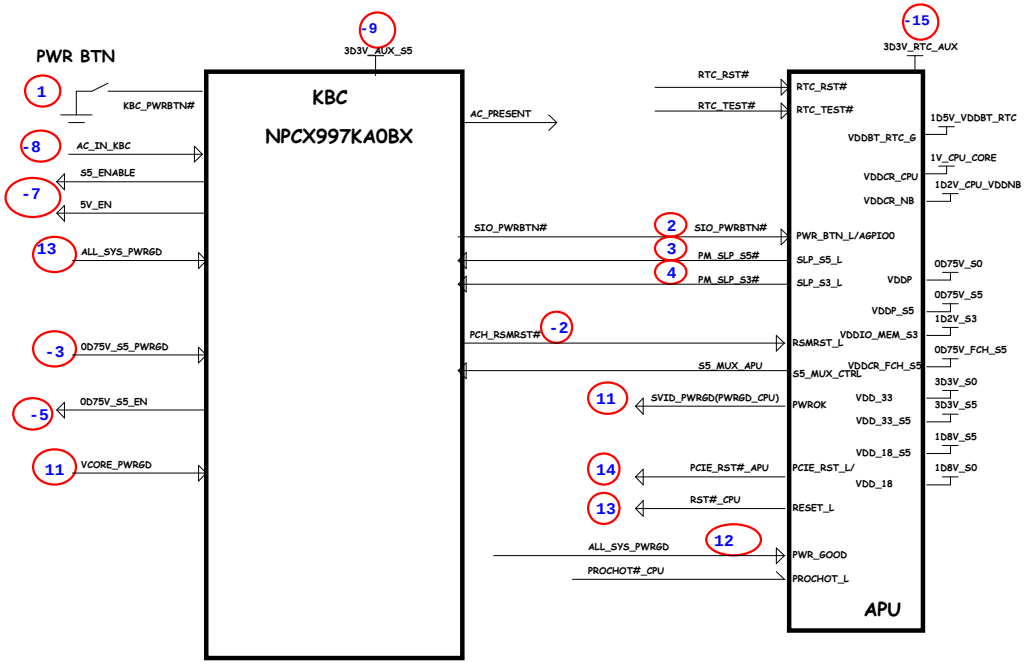
Date: Wednesday, April 06, 2022 Sheet 101 of 106

Power Sequence Block Diagram





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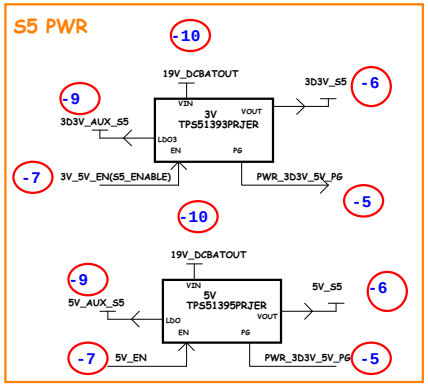

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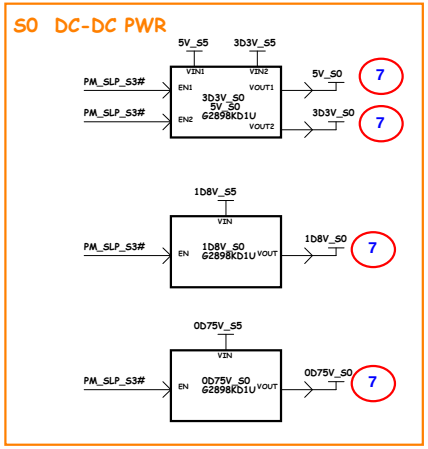
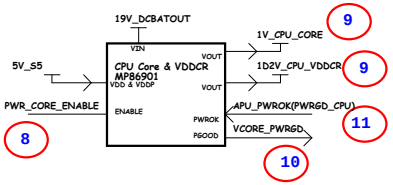


CPU Core & VDDCR



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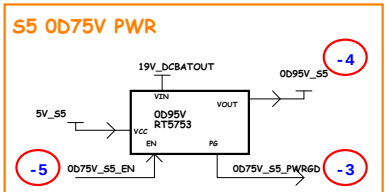

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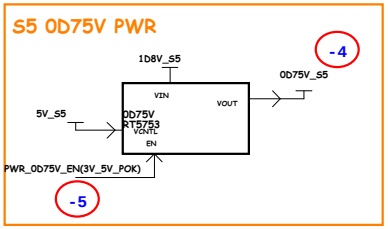

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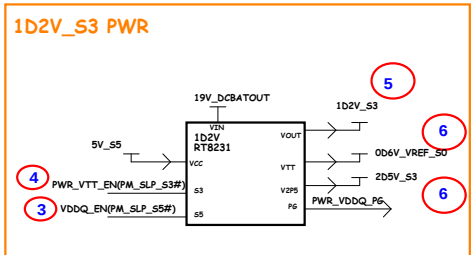

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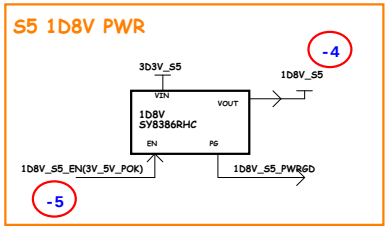

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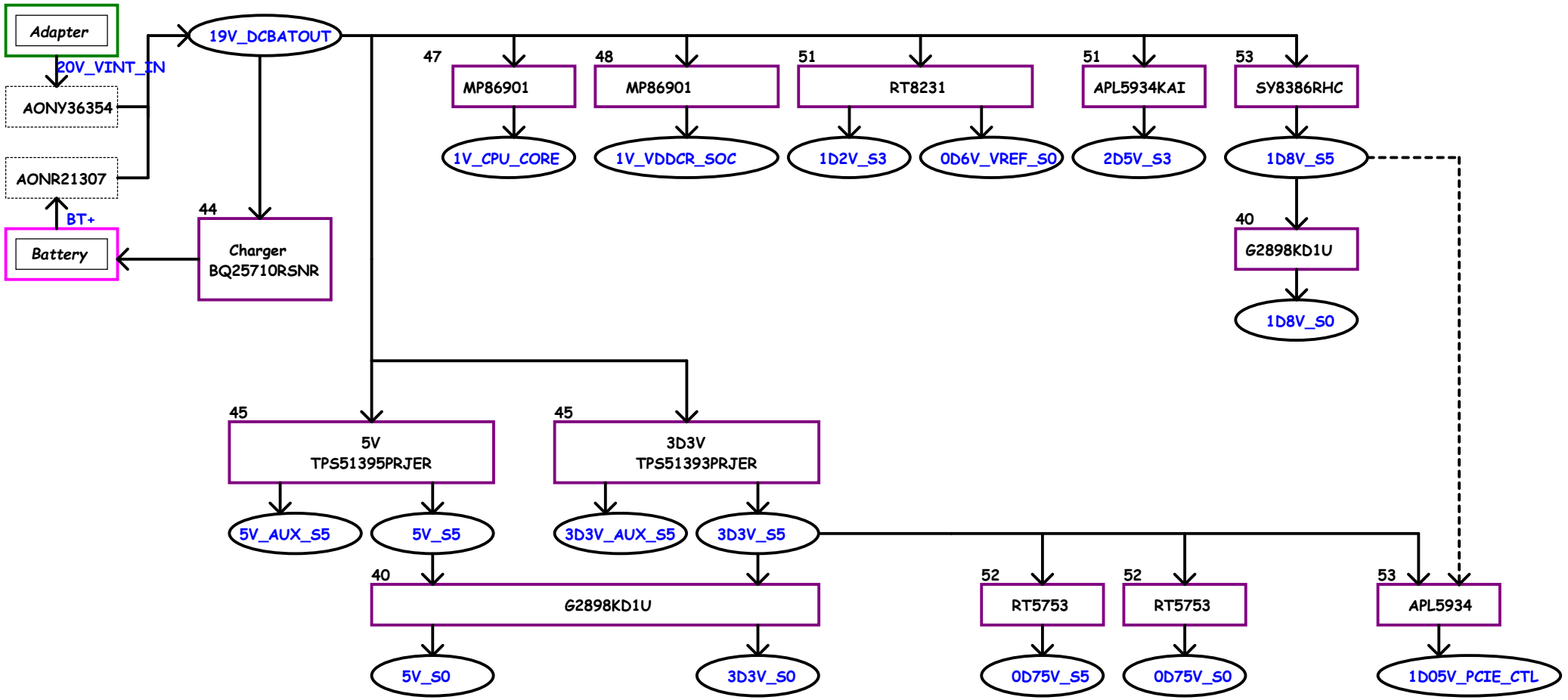
Title: POWER SEQUENCE

Size: Custom | Document Number: L14 L15 AMD | Rev: -1

Date: Wednesday, April 06, 2022 | Sheet 102 of 106



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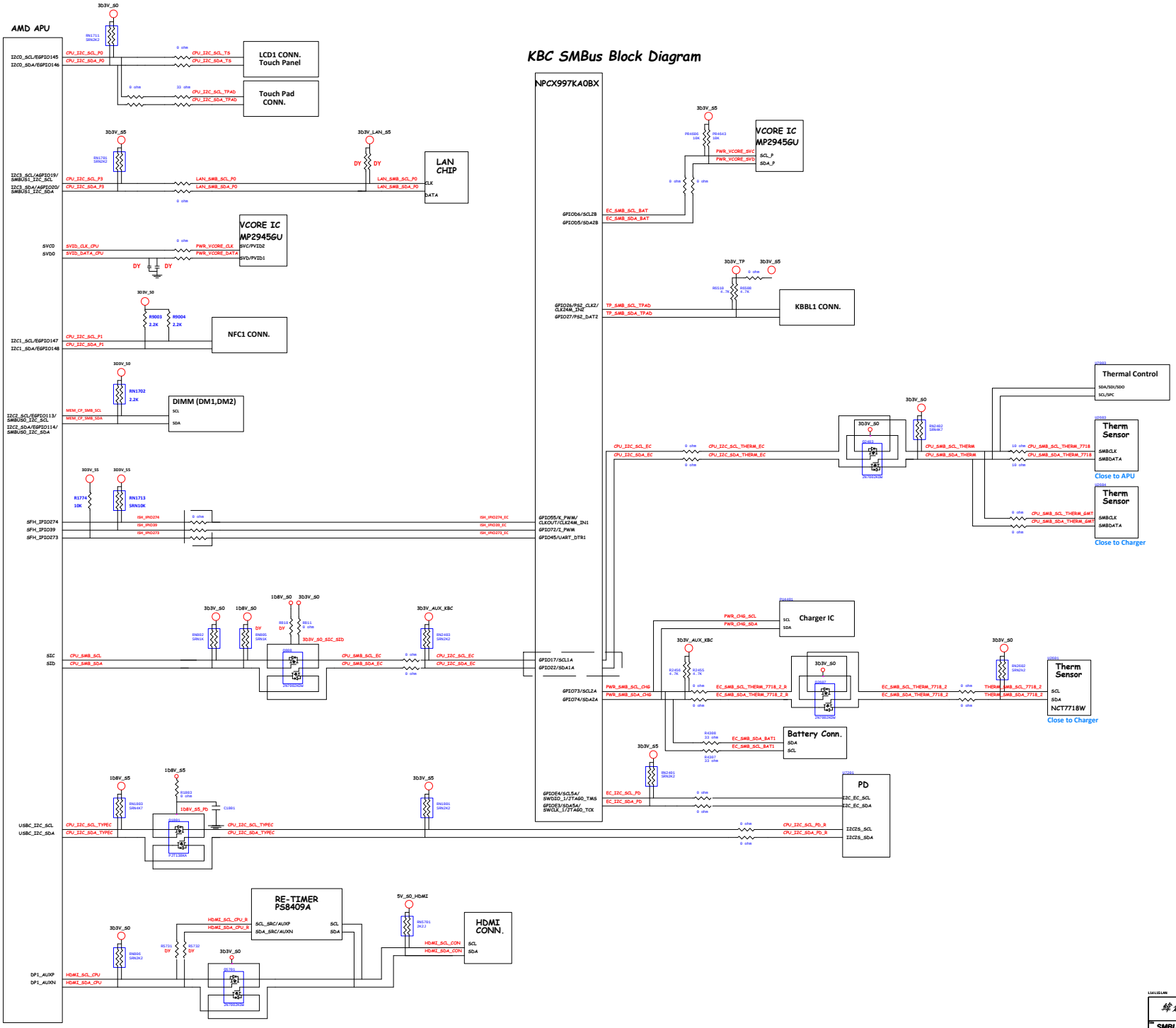
Title: POWER BLOCK DIAGRAM

Size	Document Number	Rev
A3	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 103 of 106

APU SMBus Block Diagram



KBC SMBus Block Diagram

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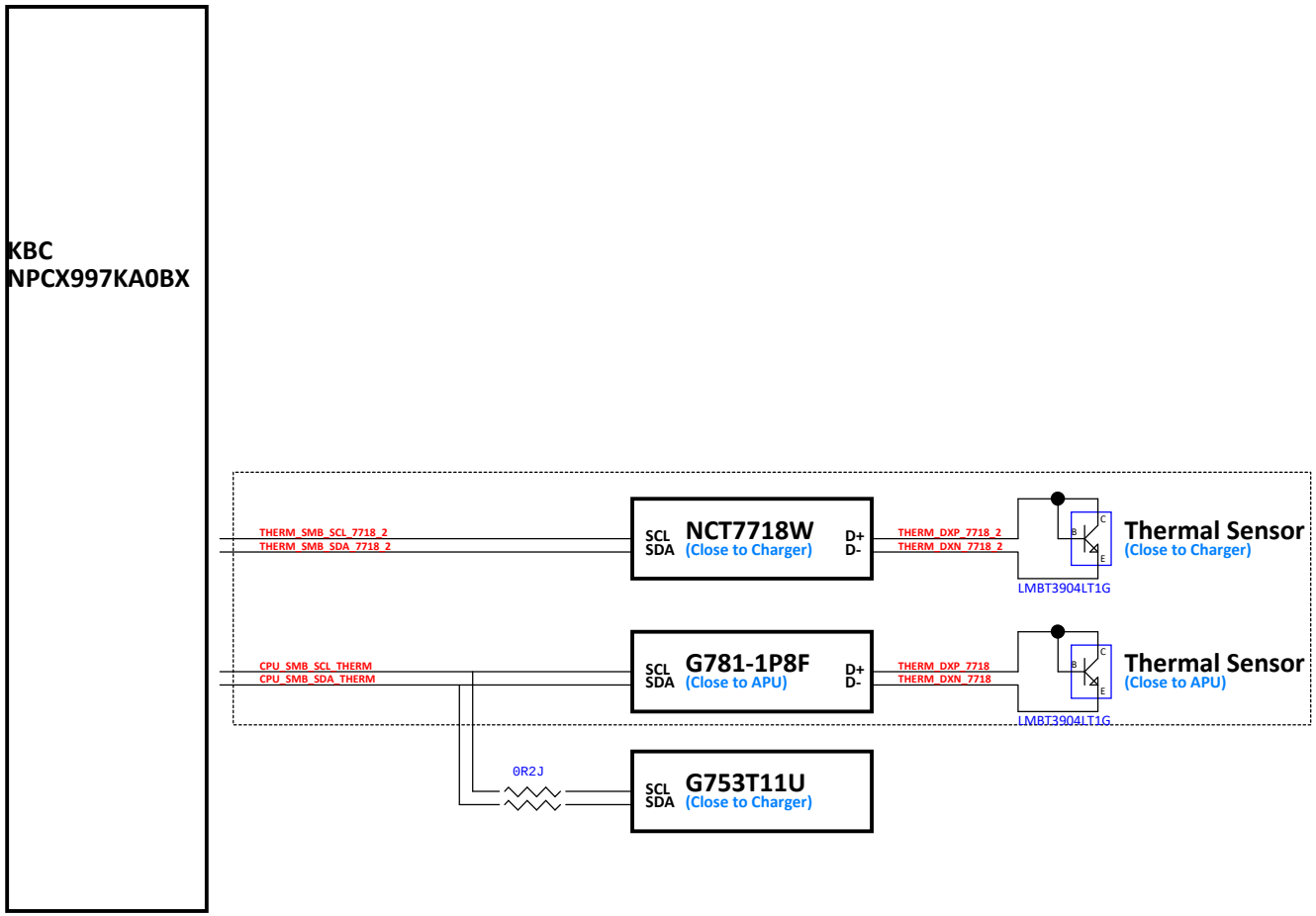
SMBUS/I2C BLOCK DIAGRAM

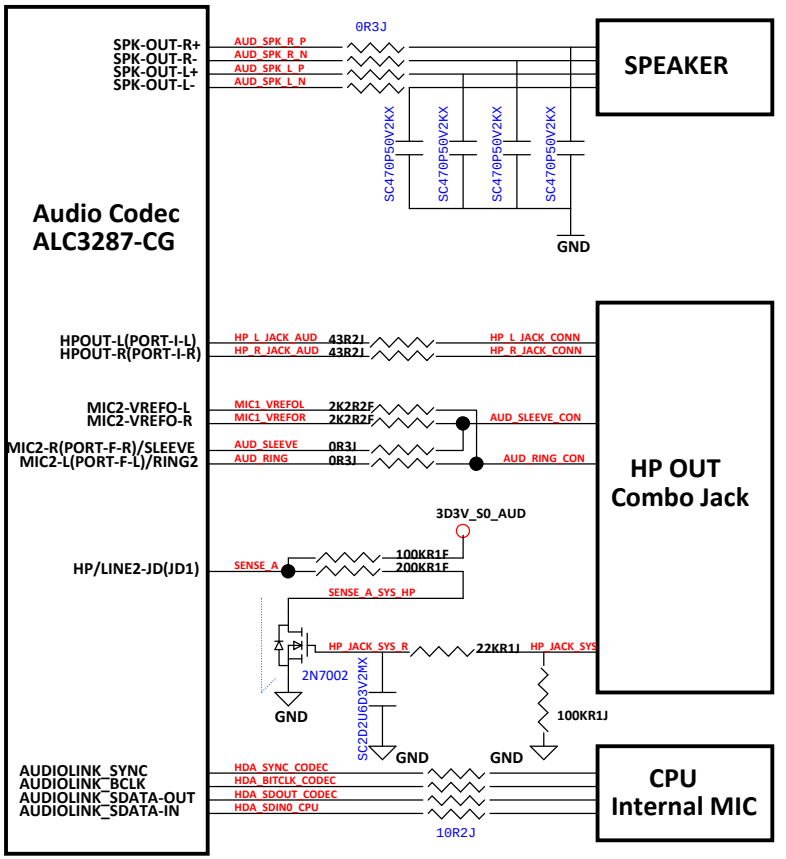
L14 L15 AMD

-1

Thermal Block Diagram



Audio Block Diagram



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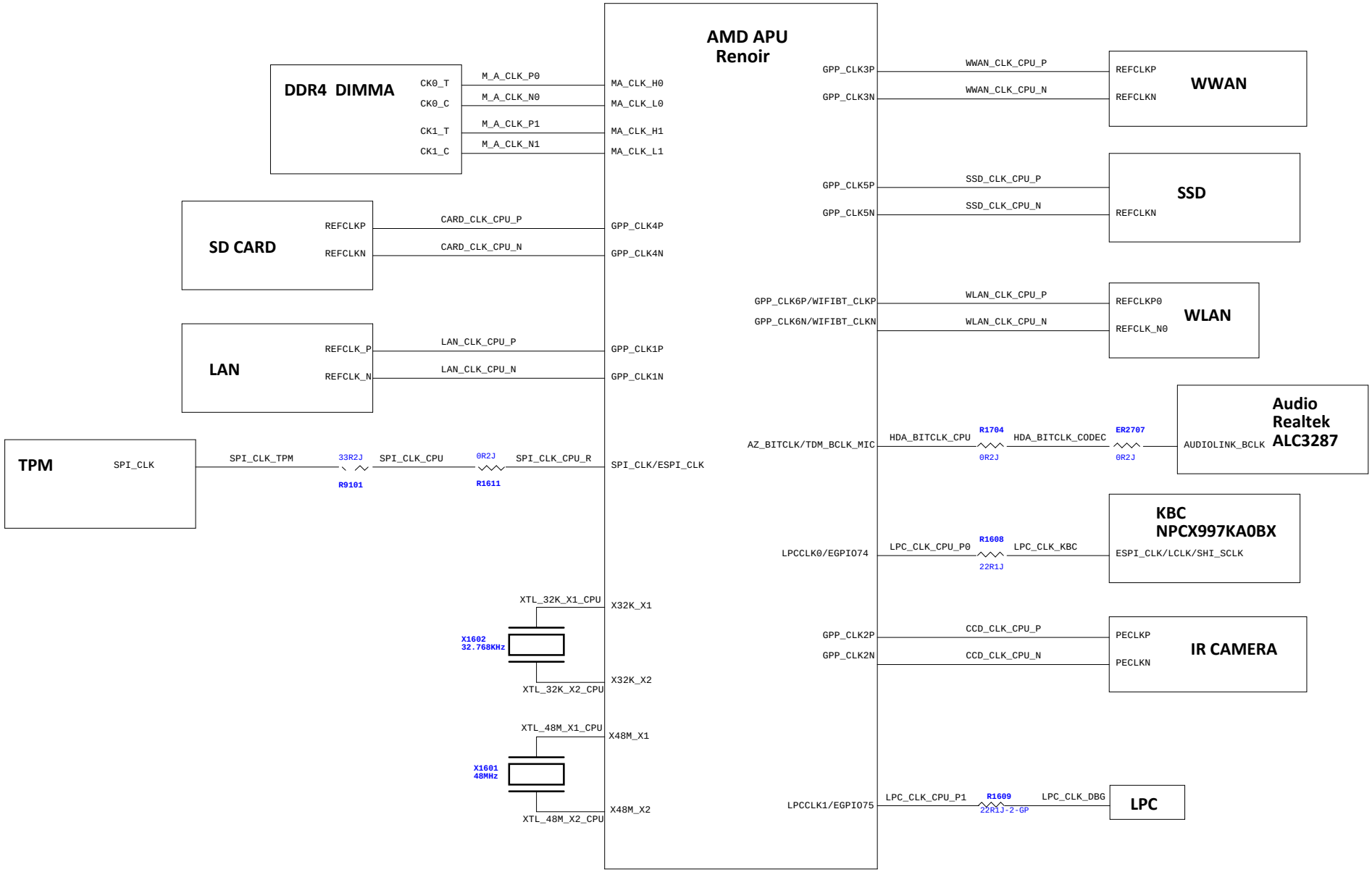
Title	THERMAL/AUDIO BLOCK DIAGRAM	
Size: Custom	Document Number: L14 L15 AMD	Rev: -1
Date: Wednesday, April 06, 2022	Sheet 105 of 106	

CLK Block Diagram



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Title: CLK BLOCK

Size	Document Number	Rev
A2	L14 L15 AMD	-1

Date: Wednesday, April 06, 2022 Sheet 106 of 106